

JITR1/R2_DDR3

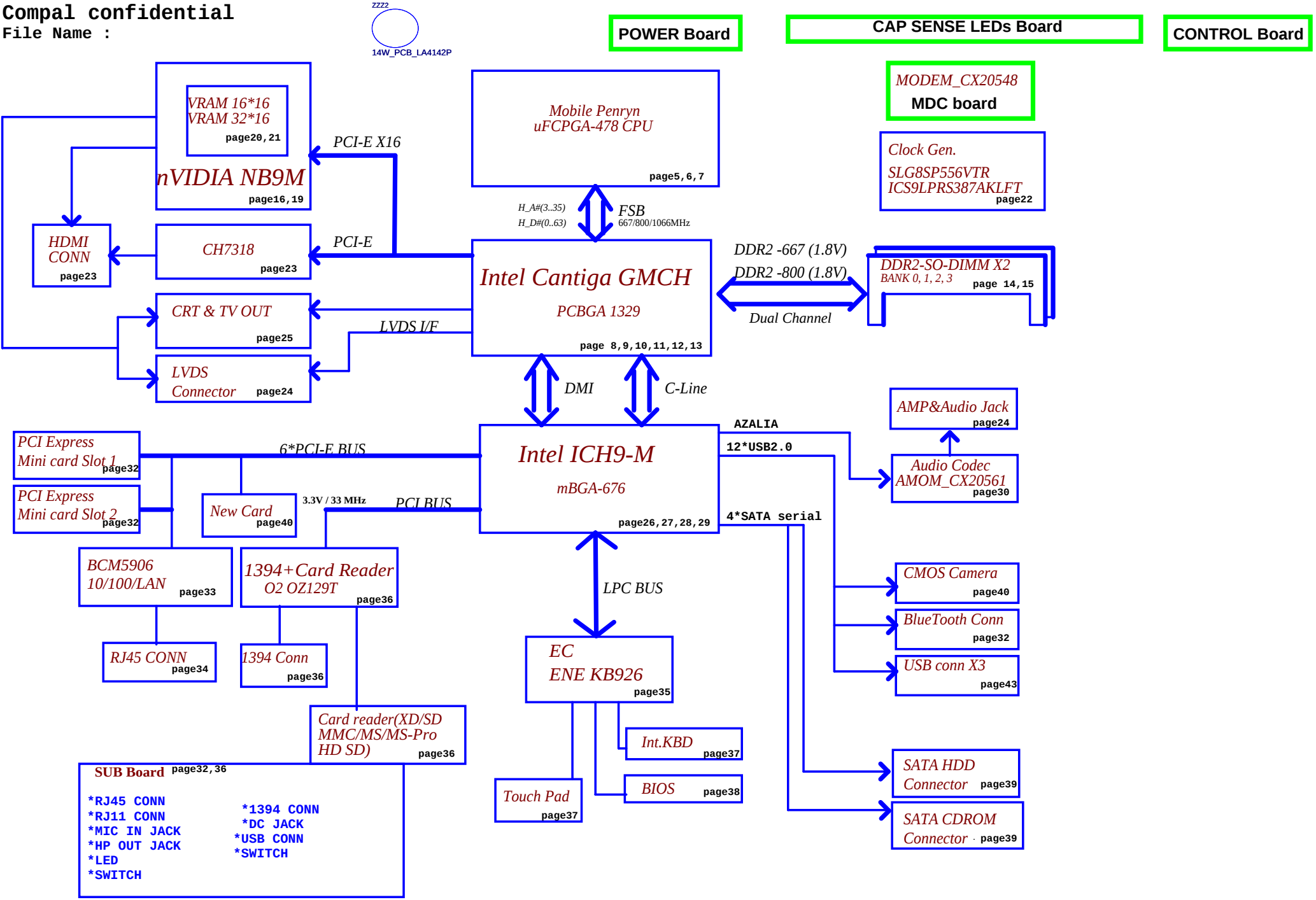
Schematics Document

Mobile Penryn uFCPGA with Intel Cantiga_GM/PM+ICH9-M core logic

Friday, April 18, 2008

REV:1.0

Security Classification	Compal Secret Data			Title Compal Electronics, Inc.		
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Size Custom		
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				Date:		Sheet 1 of 52



DDR2 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

DDR3 Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
S0	0	0	0	0
S1	0	0	0	0
S3	0	0	0	X
S5 S4/AC	0	0	X	X
S5 S4/ Battery only	0	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_S0_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_S0 SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

VGA and DDR2 Voltage Rails (NB9M-GS)

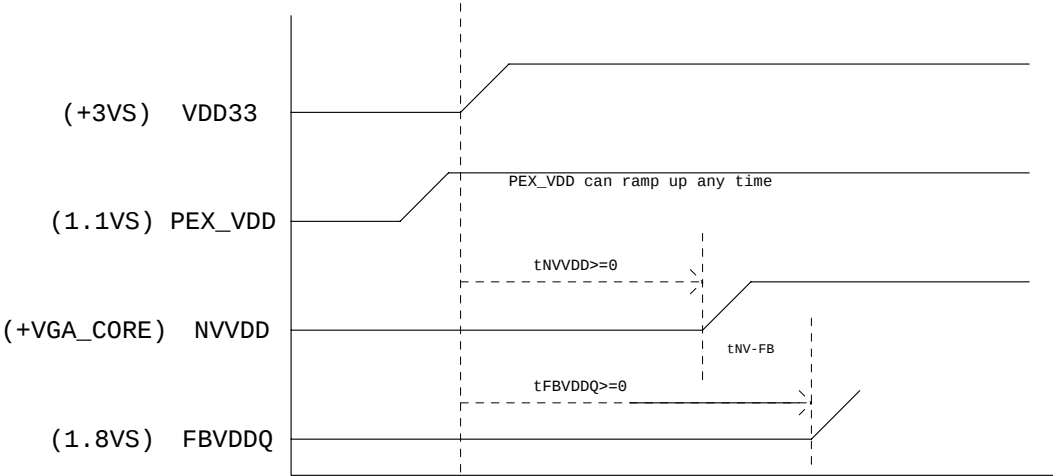
State \ power plane			+1.8V	+3VS +VGA_CORE
	S0	0	0	0
	S1	0	0	0
	S3	0	0	X
	S5 S4/AC	0	0	X
	S5 S4/ Battery only	0	X	X
	S5 S4/AC & Battery don't exist	X	X	X

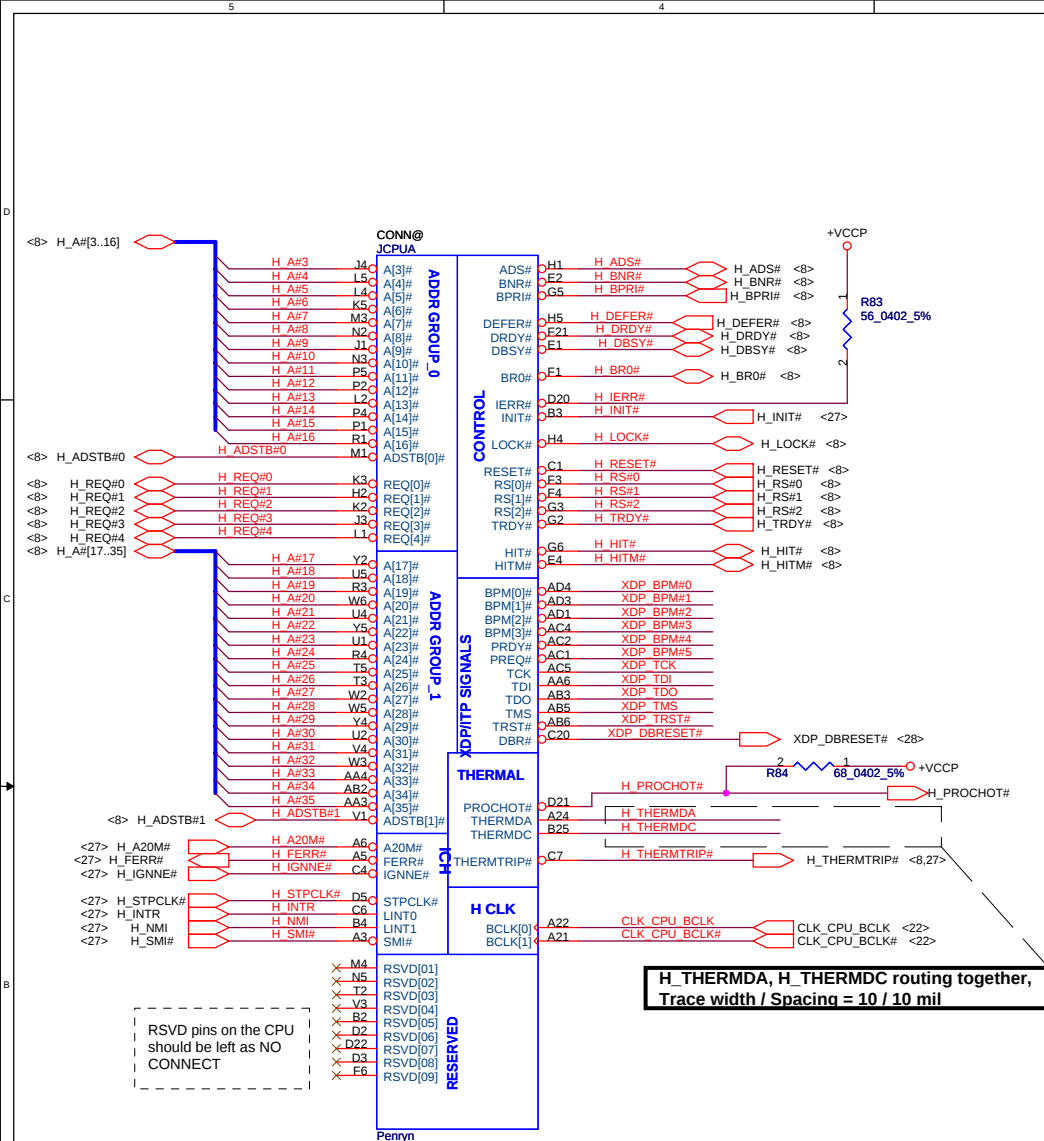
EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDD	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVD	1.1	55mA			
SP_PLLVDD	1.1	25mA			
VID_PLLVDD	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDD/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDD	1.8	100mA			
IFPCD_PLLVDD	1.8	160mA			
IFPEF_PLLVDD	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

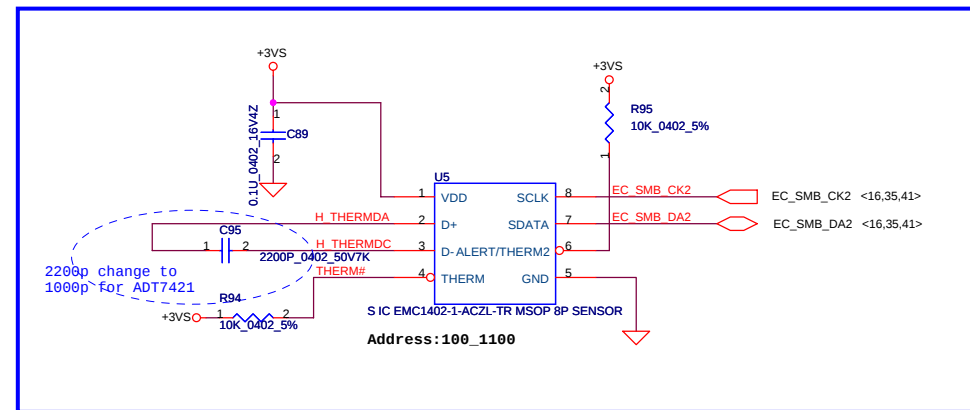
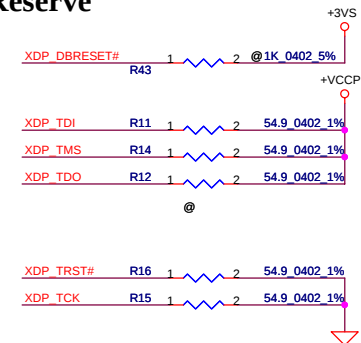
POWER SQUENCE

The ramp time for any rail must be more than 40us

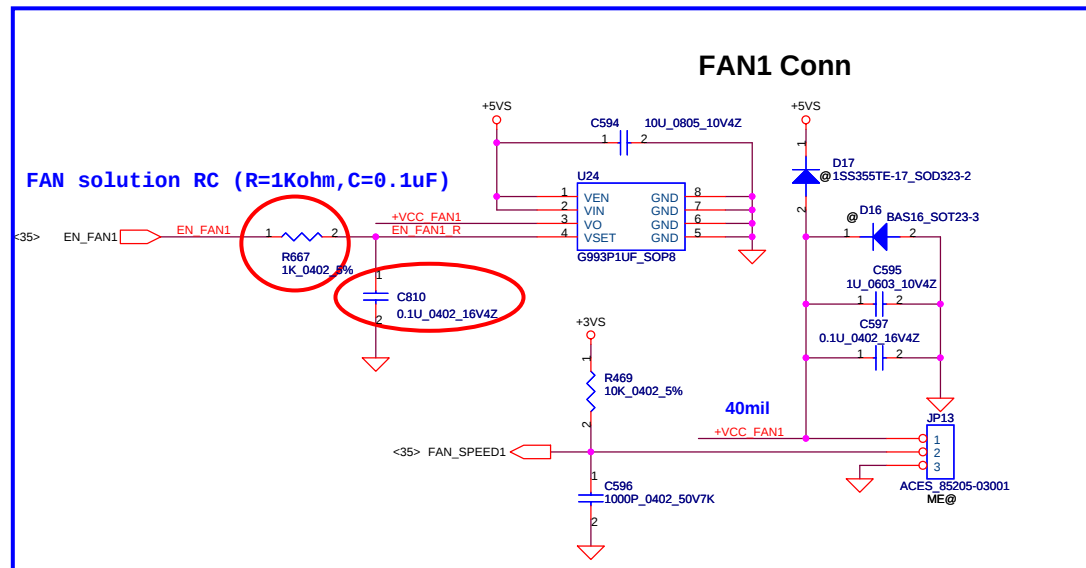




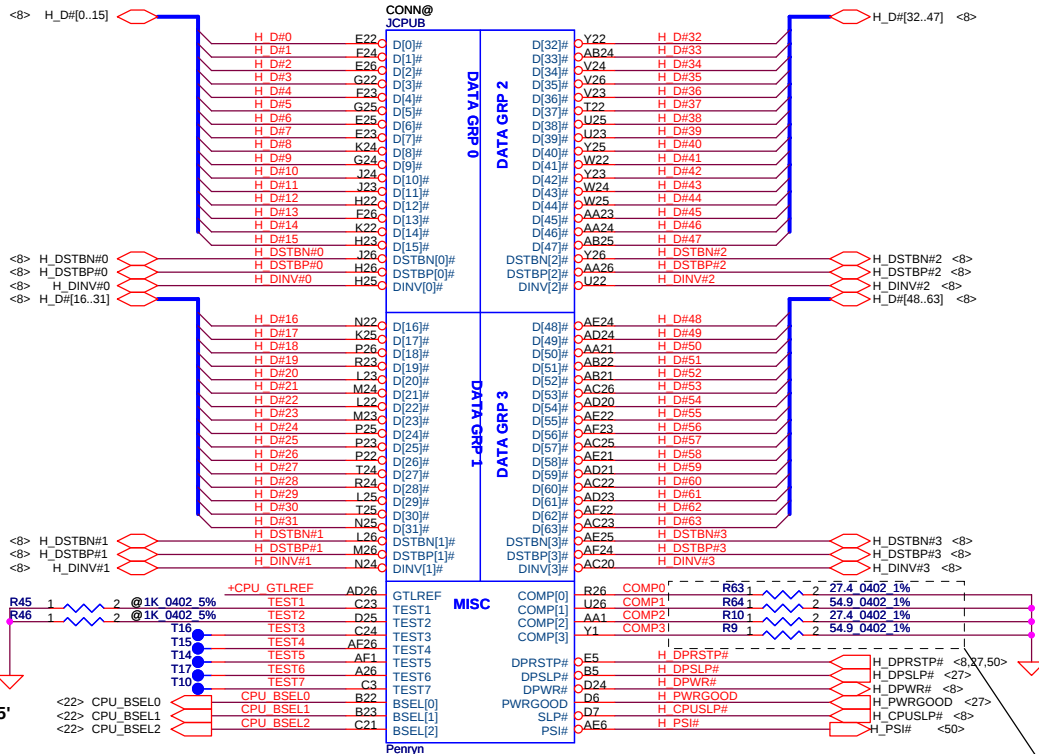
XDP Reserve



FAN1 Conn

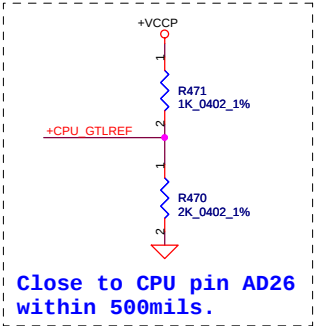


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				JITR1_LA-4141P	
				Date: Friday, May 02, 2008	Rev 0.1
				Sheet 5	of 52



Width=4 mil ,
Spacing: 15mil
(55Ohm)

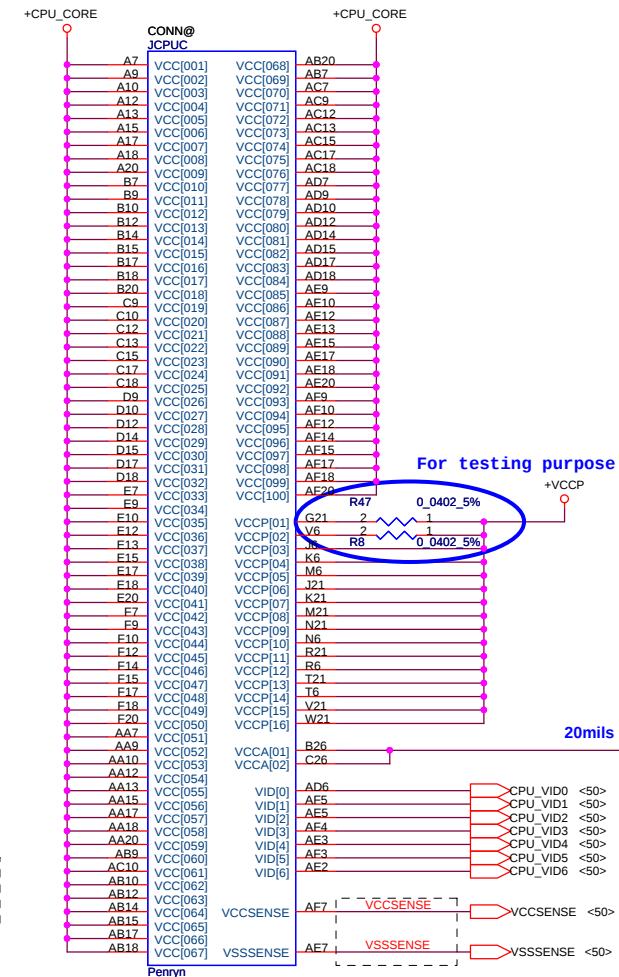
Layout note: Z0=55 ohm
0.5" max for GTLREF.



layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

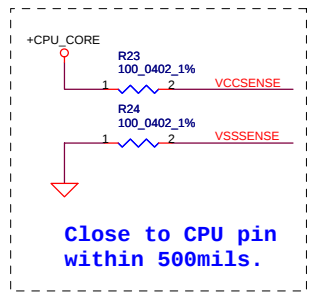
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

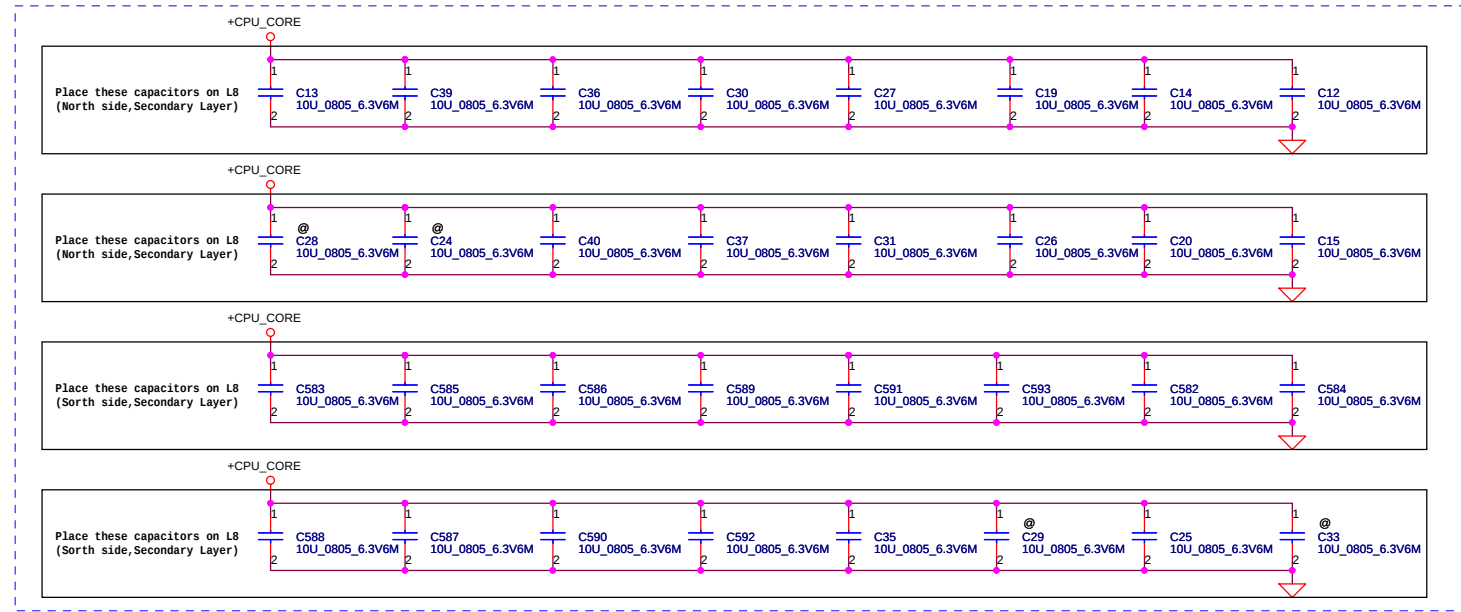
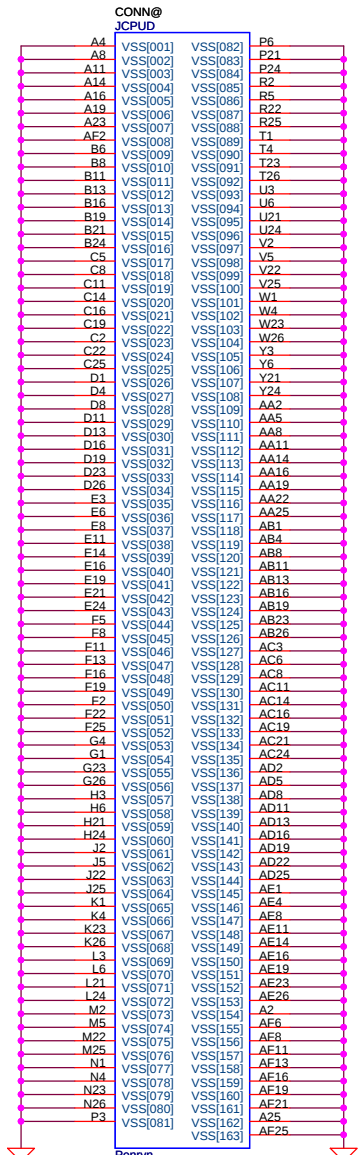
TRACE CLOSELY CPU < 0.5"
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)



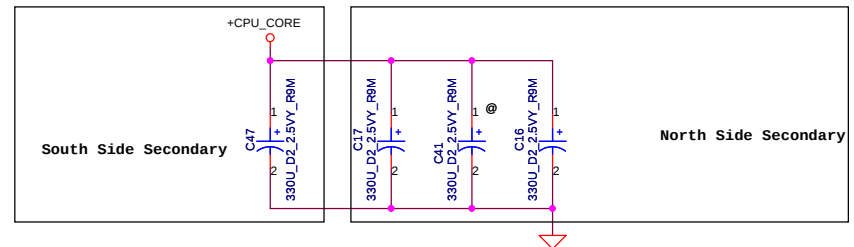
Length match within 25 mils.
The trace width/space/other is 16/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

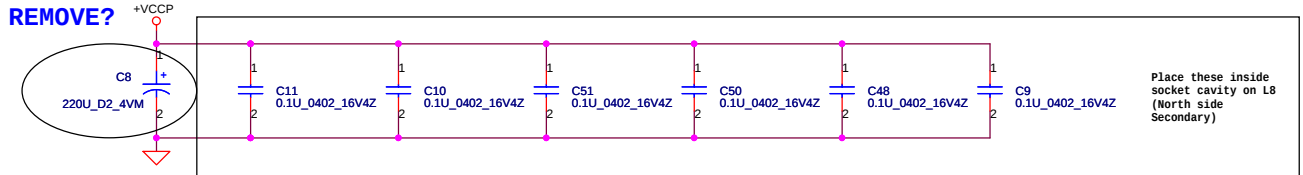


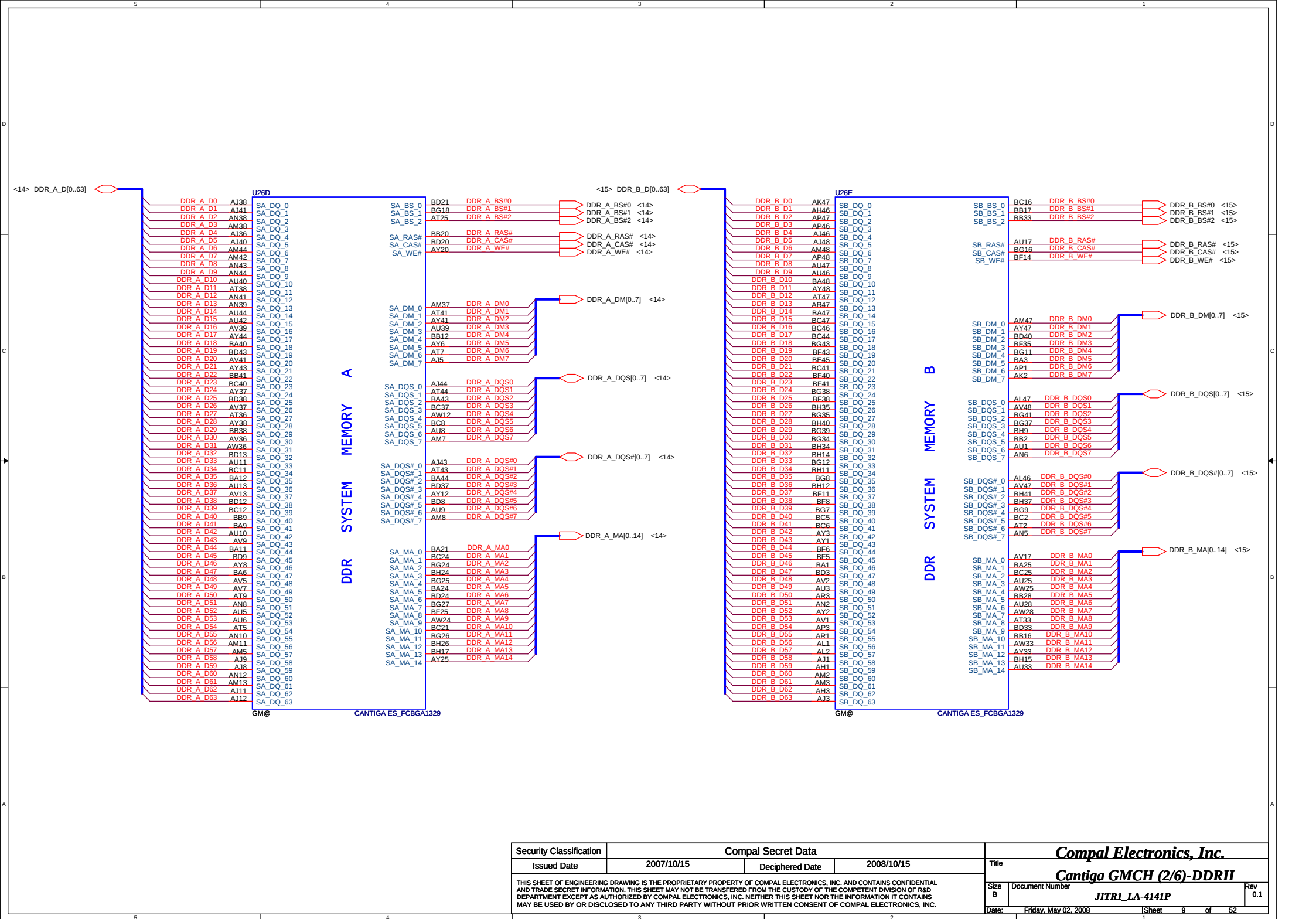


Mid Frequency Decoupling



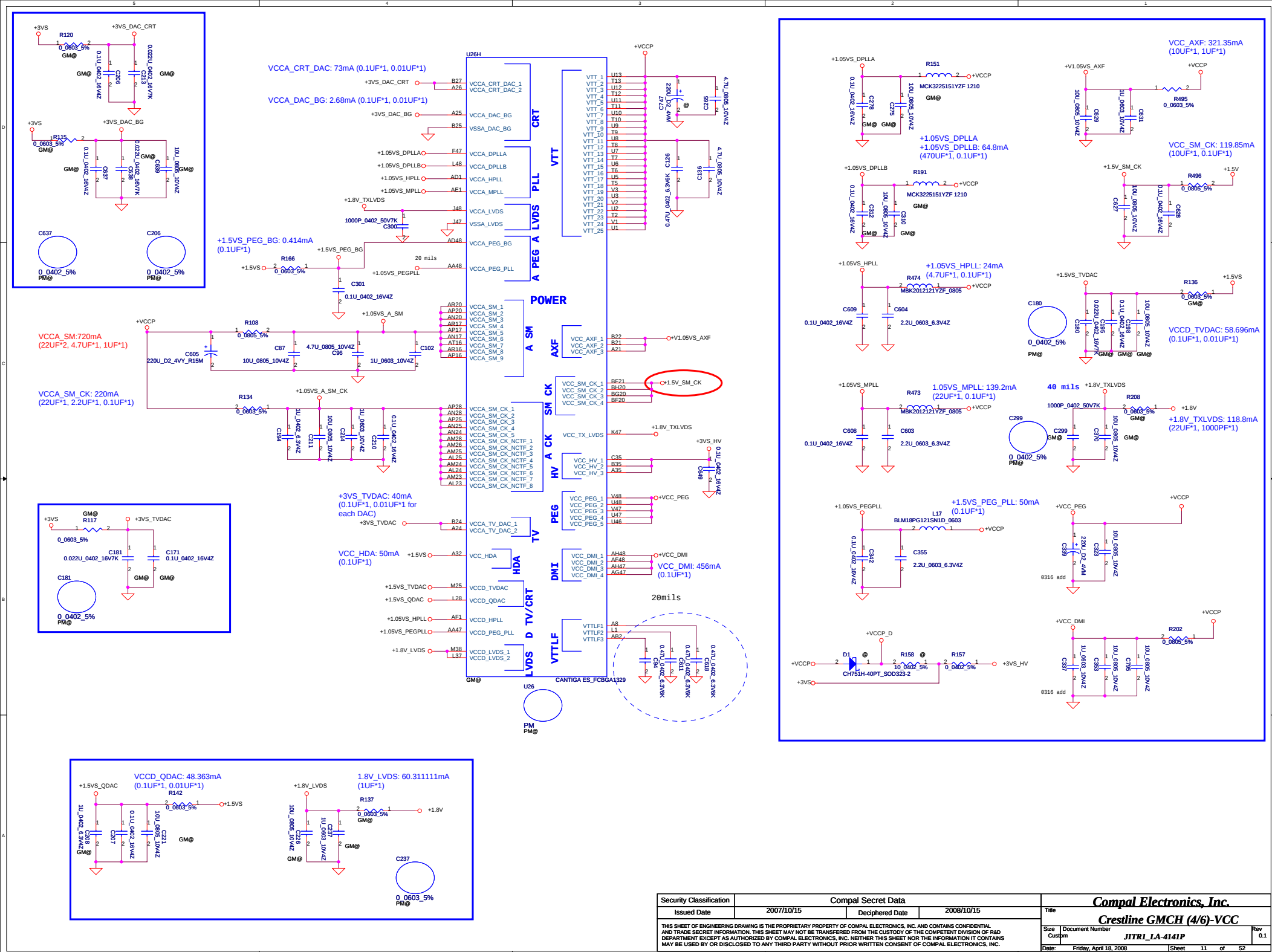
ESR <= 1.5m ohm
Capacitor > 1980uF



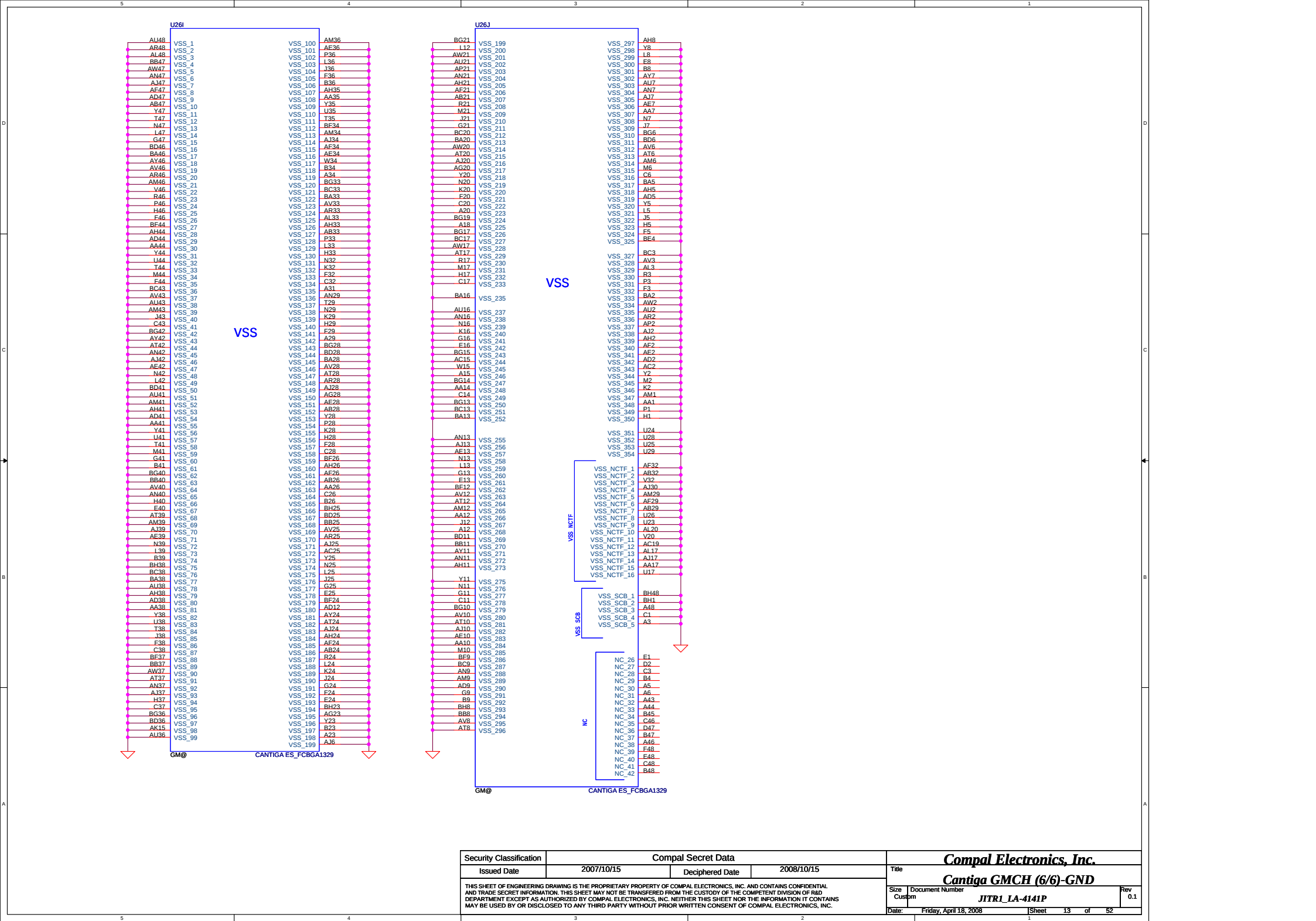


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		Size	Document Number	Rev	
		B	Friday, May 02, 2008	0.1	
Date:		Friday, May 02, 2008	Sheet	9	of 52

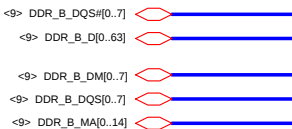




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				Date:	Friday, April 18, 2008	Sheet 11 of 52

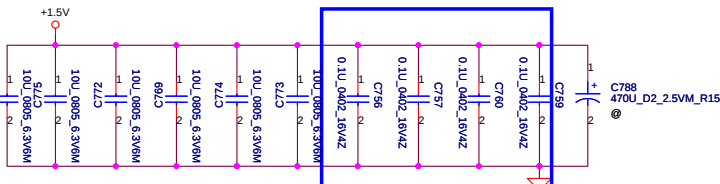


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				Custom	0.1
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				Date:	Friday, April 18, 2008
				Sheet	13 of 52

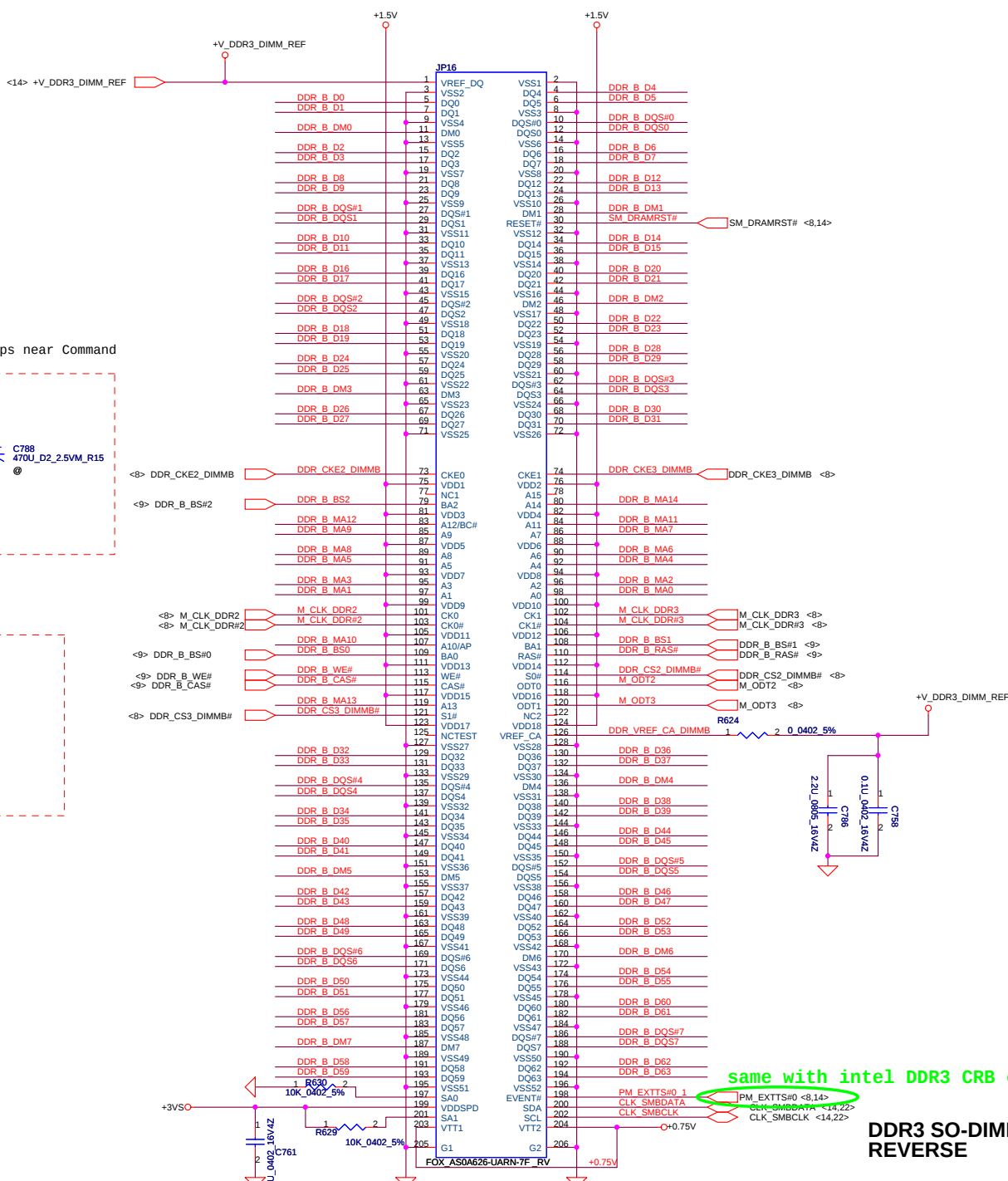
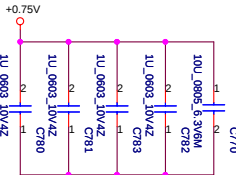


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command
and Control signals of DIMMA



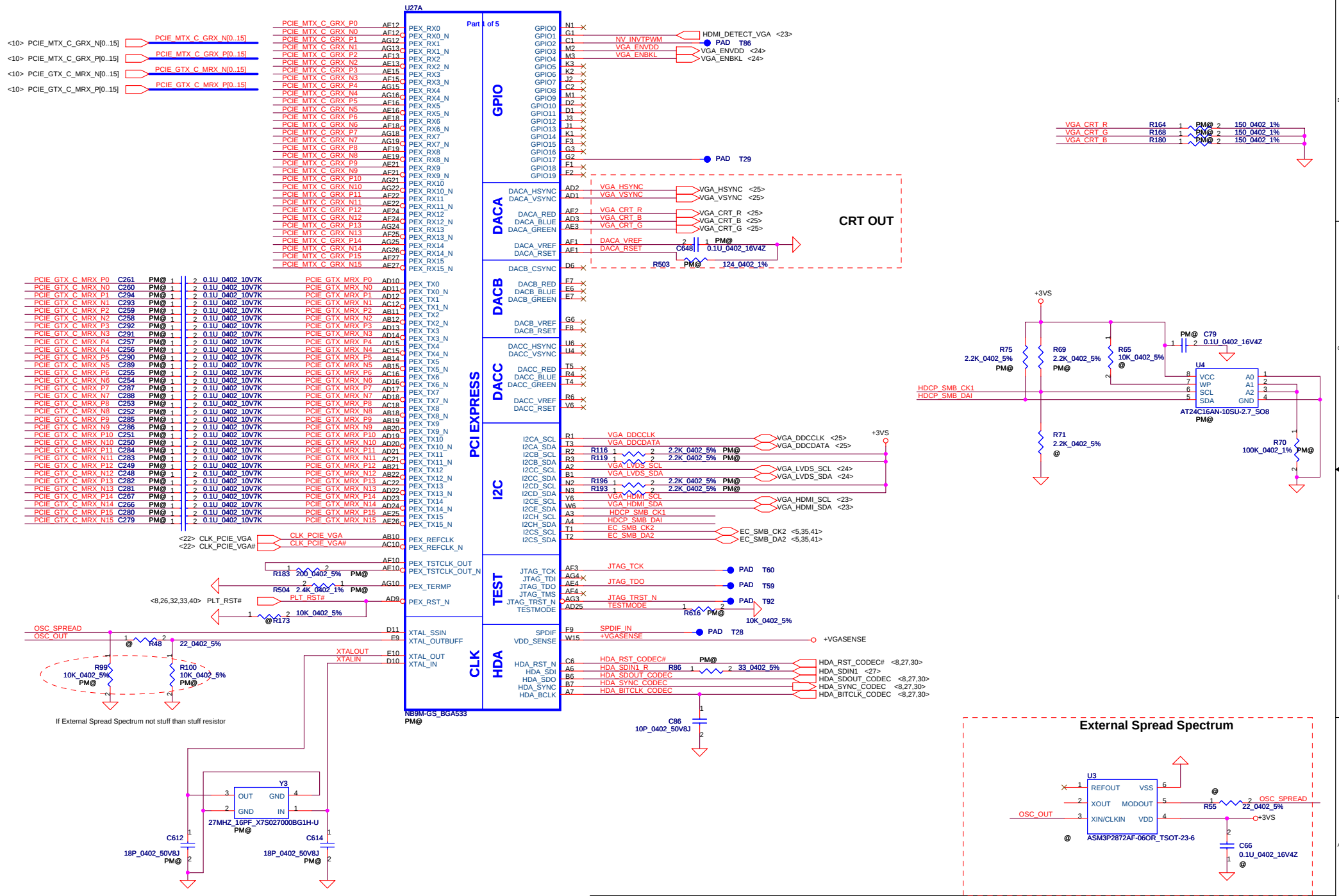
Layout Note:
Place near JP5.203 & JP5.204



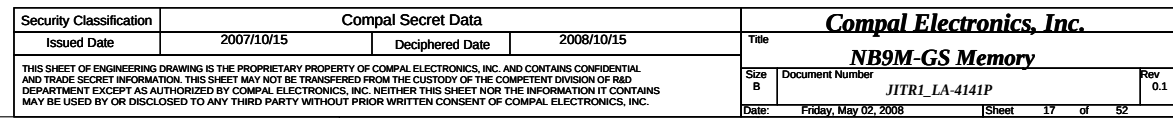
same with intel DDR3 CRB connection

DDR3 SO-DIMM B
REVERSE

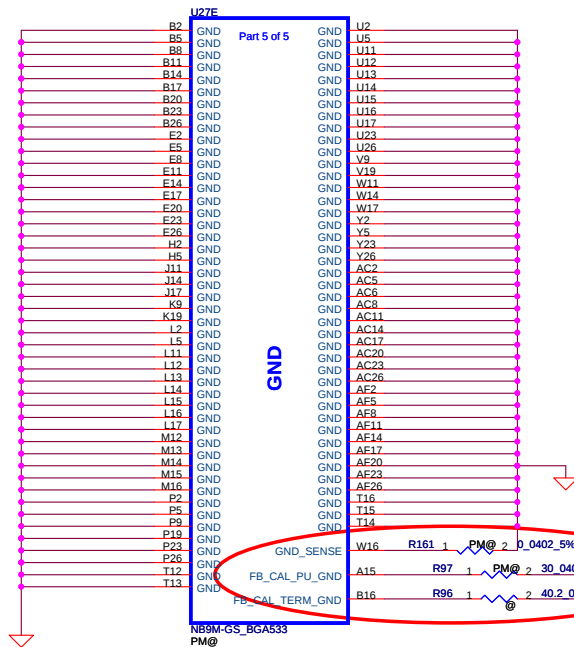
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				Size	Document Number
				Montevina UMA DDR3	
				Date	Rev
				Friday, May 02, 2008	1.0
				Sheet	15 of 52



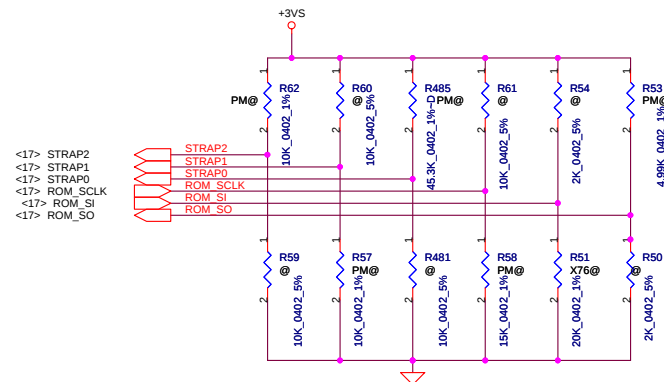
Security Classification		Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	NB9M-GS PCIE, LVDS, GPIO, CLK	
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Date: Wednesday, May 07, 2008				Sheet 16	of 52



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				Custom			0.1
				Date:	Monday, May 05, 2008	Sheet	18



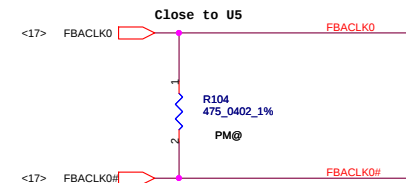
A total of 8 signals are required for GB1 strapping this includes
 2 reference signals
 6 physical strapping pins
 4 logical strapping bits
 A total of 24 logical strapping bits are available



GB1 Family GPU Strap Options

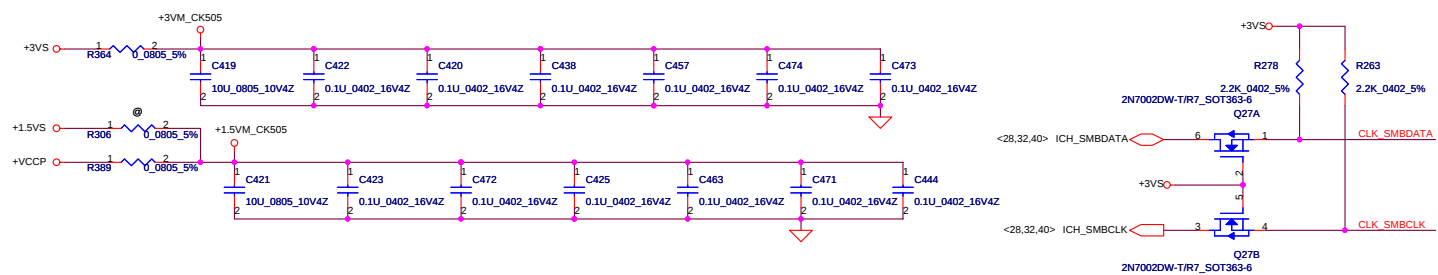
GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(5)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K

Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (32M*16)	Hynix	SA000012G30	X7611338L04
	Qimonda	SA00001YF10	X7611338L05
	Samsung	SA00001KH10	X7611338L06

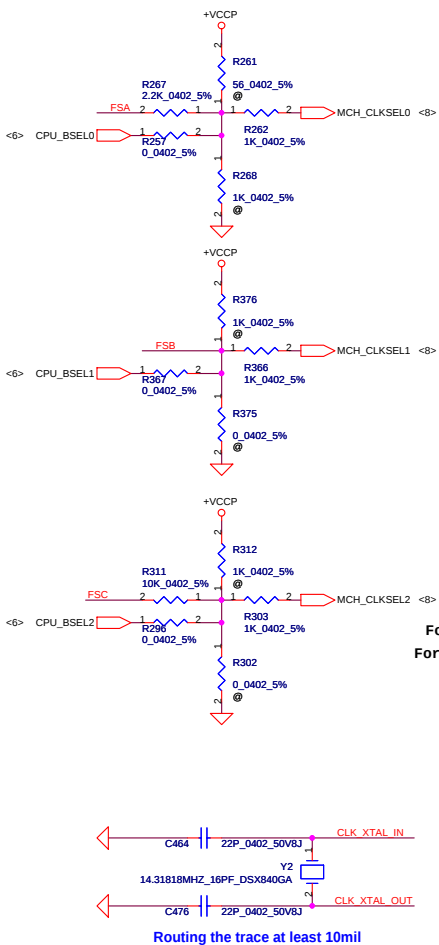


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				Document Number	0.1
				Custom	
				JITRI_LA-4141P	
Date: Friday, May 02, 2008				Sheet 20 of 52	

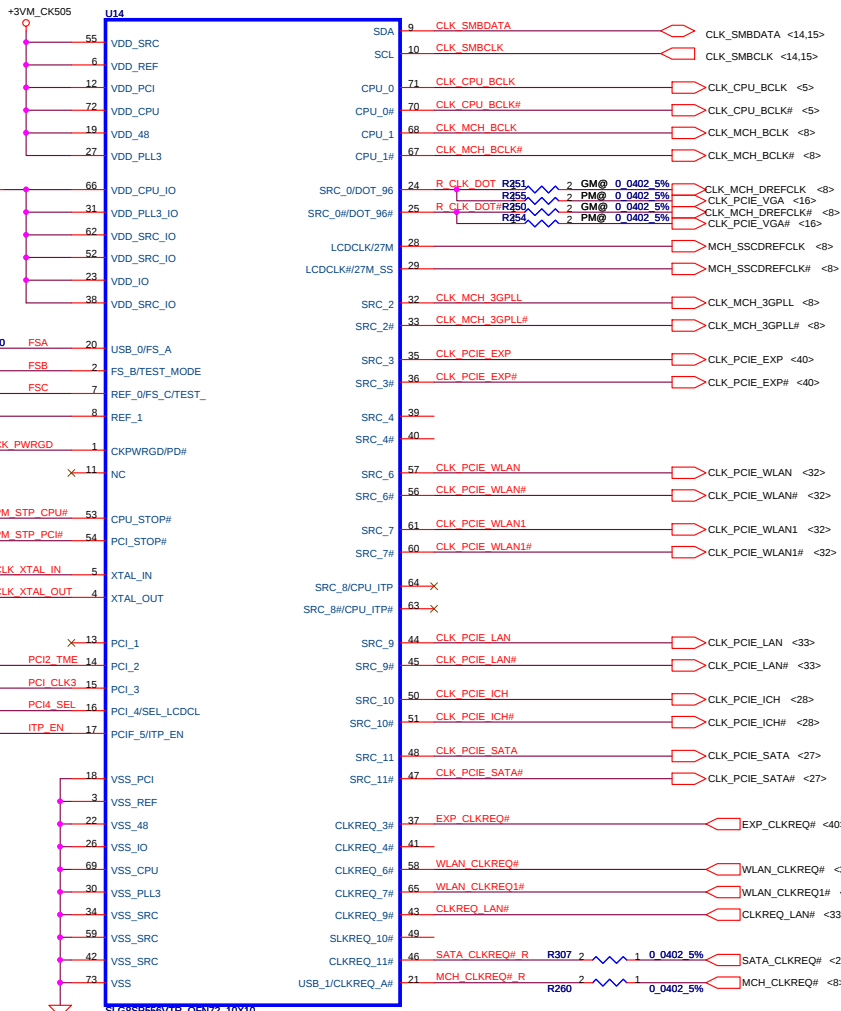
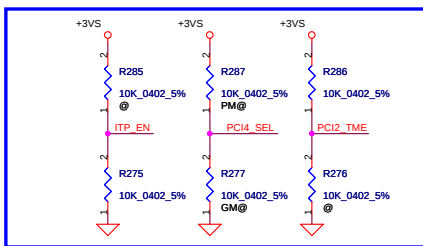
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS



SRC PORT LIST

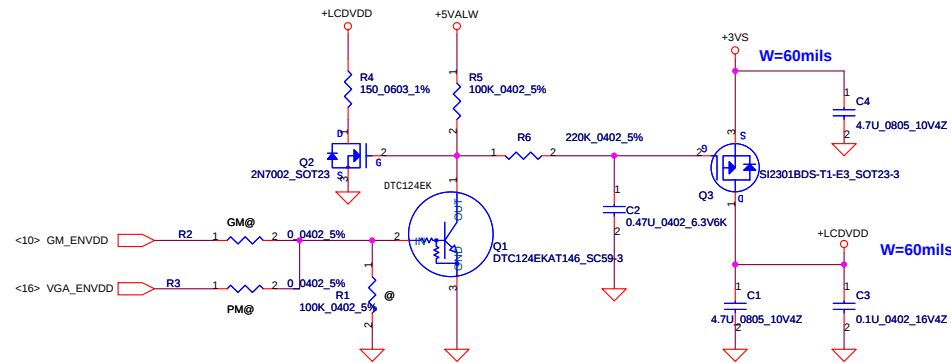
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	PCIE_WLAN
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

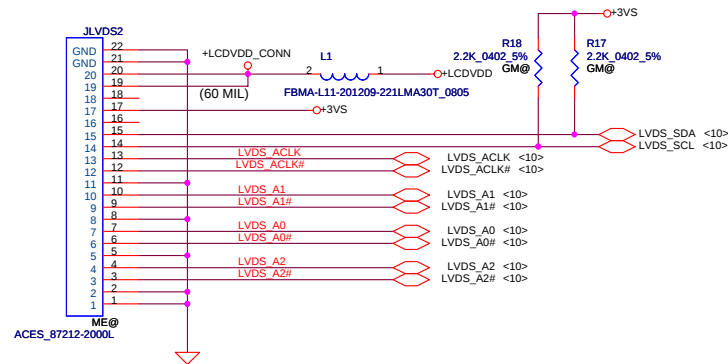
PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

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				Date	Monday, May 05, 2008
				Sheet	22 of 52

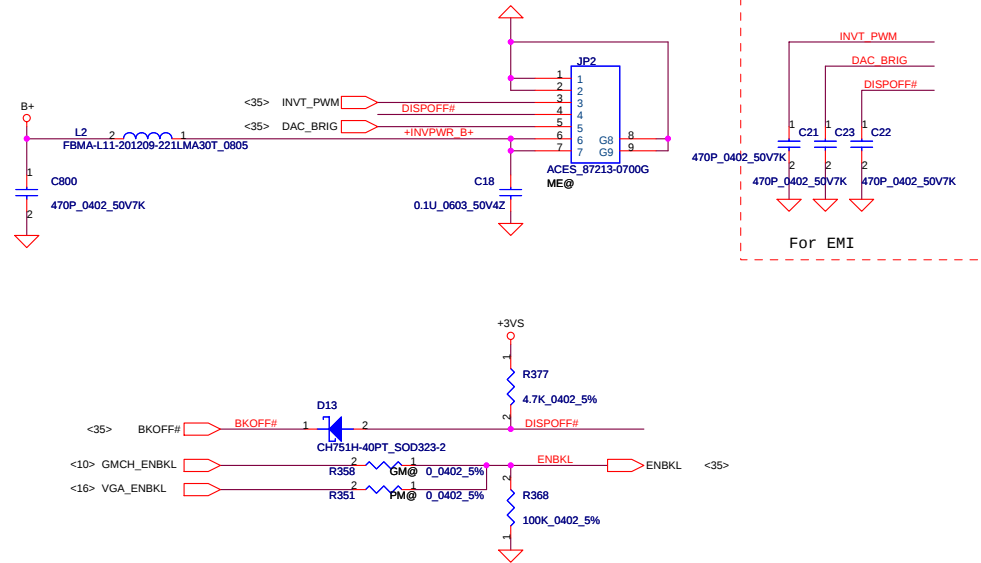
LCD POWER CIRCUIT



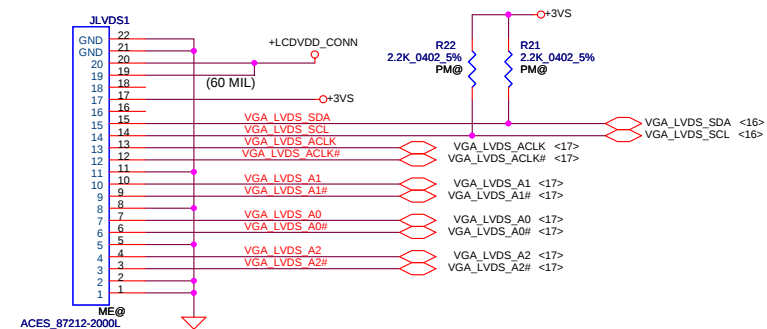
LCD/PANEL BD. Conn.



INVERTER Conn.



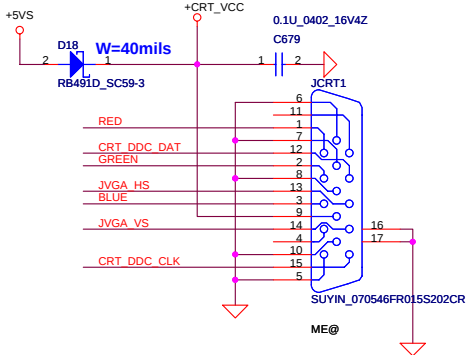
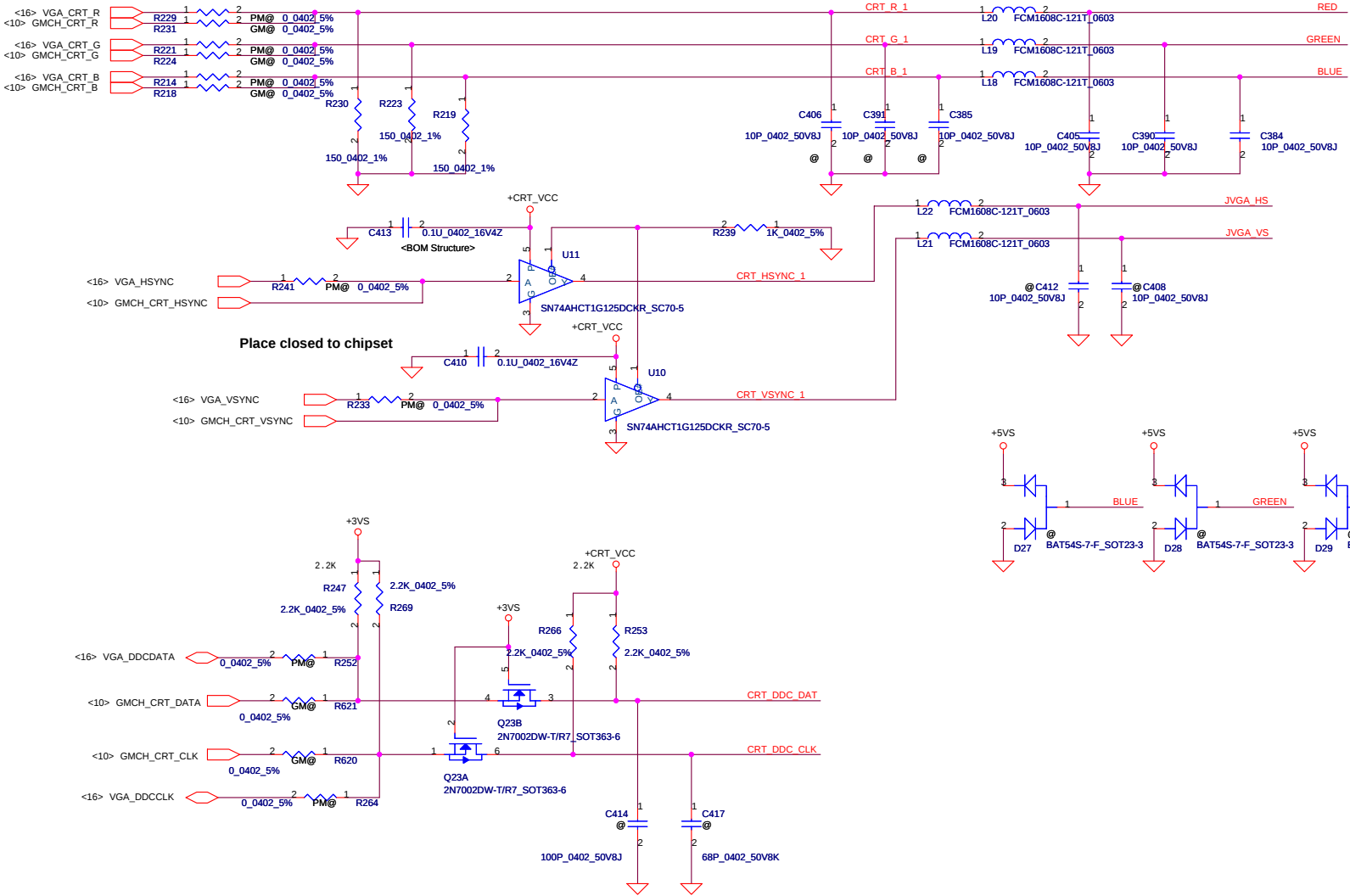
LCD/PANEL BD. Conn.



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Size	Document Number	JITRI_LA-4141P		Rev	0.1
Date:	Friday, May 02, 2008	Sheet	24	of	52

CRT Connector

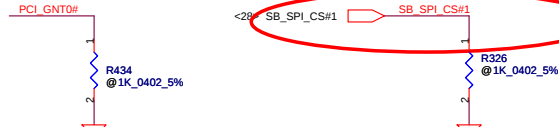
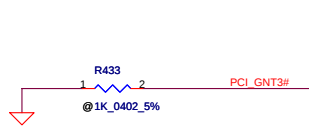
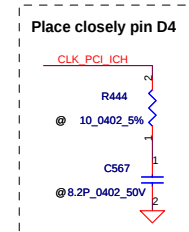
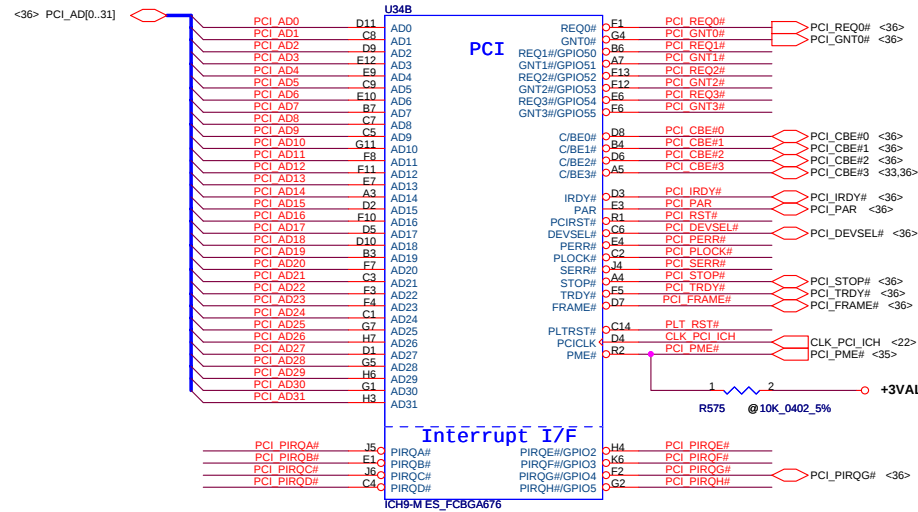
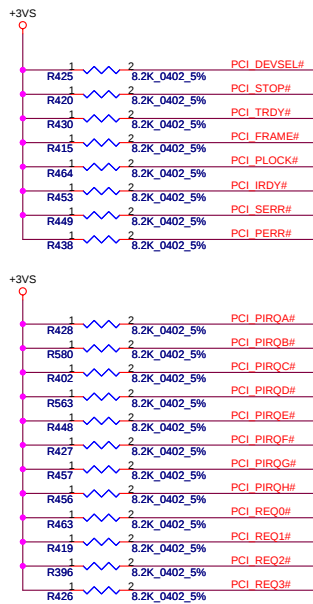
Place closed to chipset



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

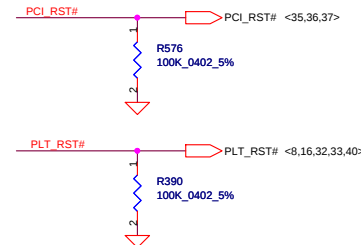
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Size	Custom	Document Number	JITR1_LA-4141P	Rev 0.1
Date:	Friday, May 02, 2008	Sheet	25	of 52

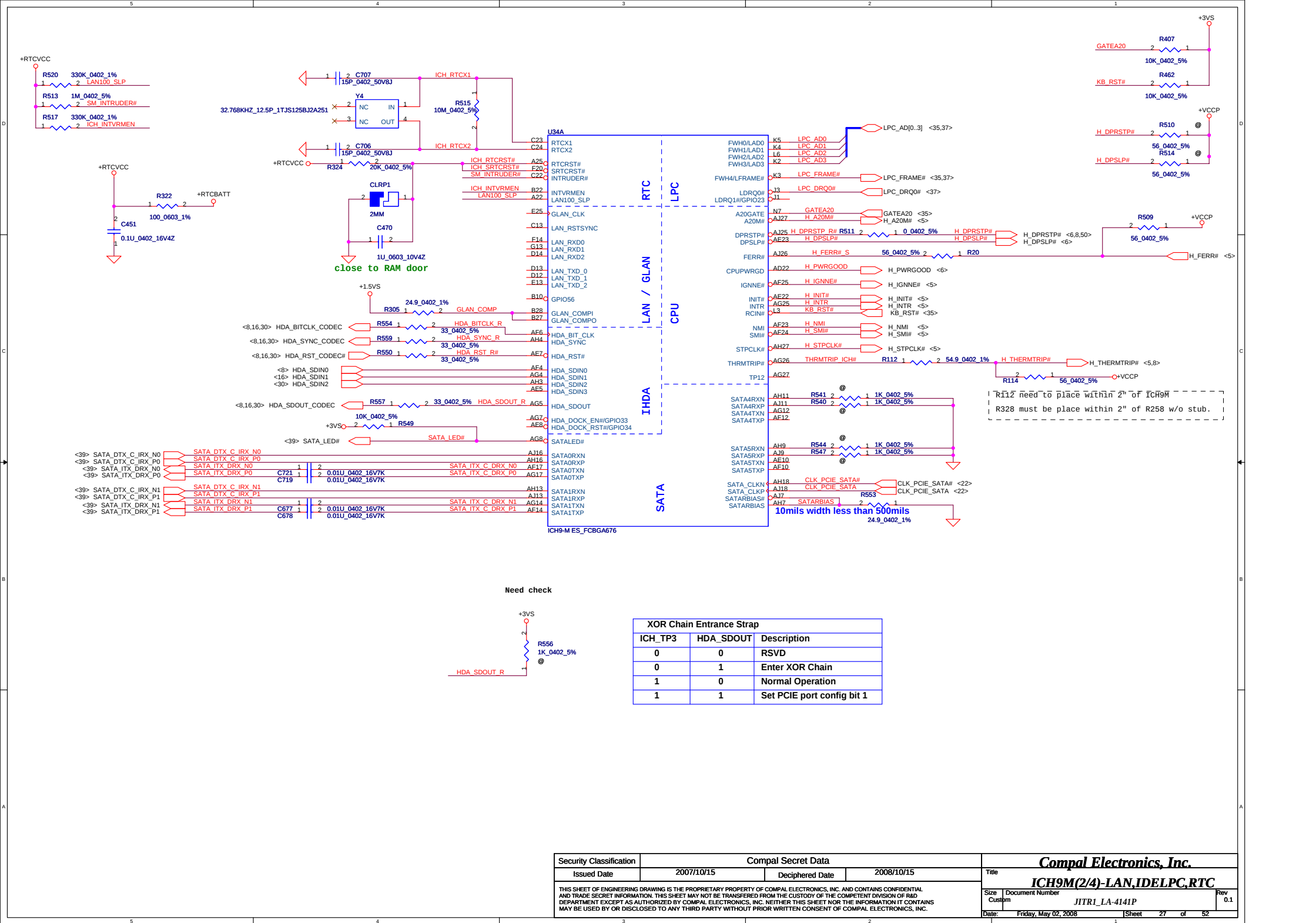


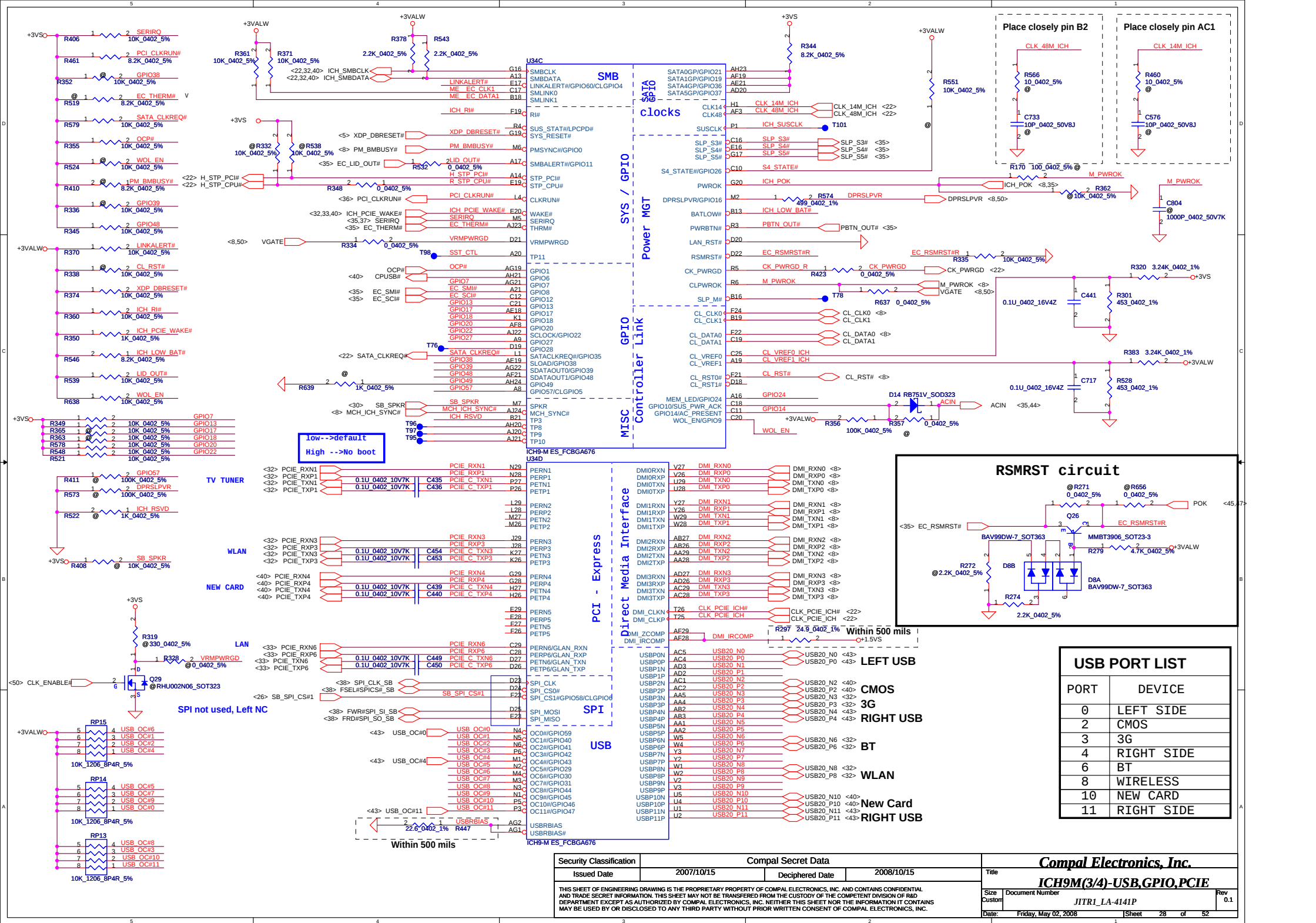
Pull high?

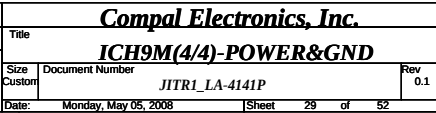
A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*









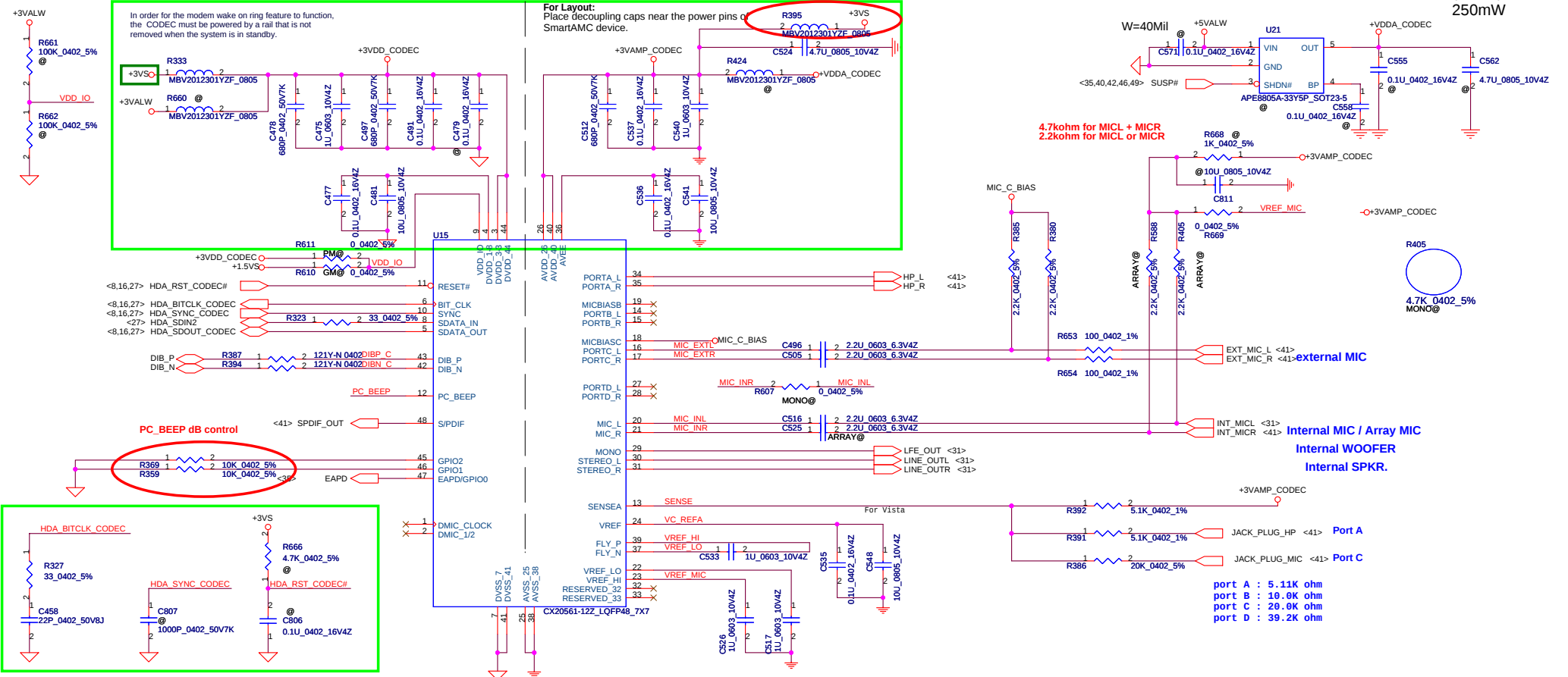
AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680p

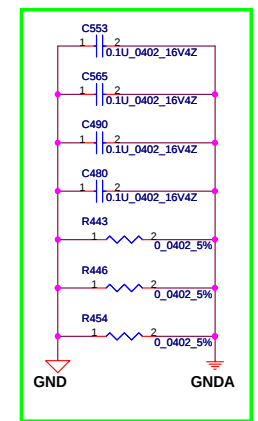
CHANGE TO 0ohm (2008/05/05)

CODEC POWER

(3.33V)
250mW



DIGITAL ANALOG



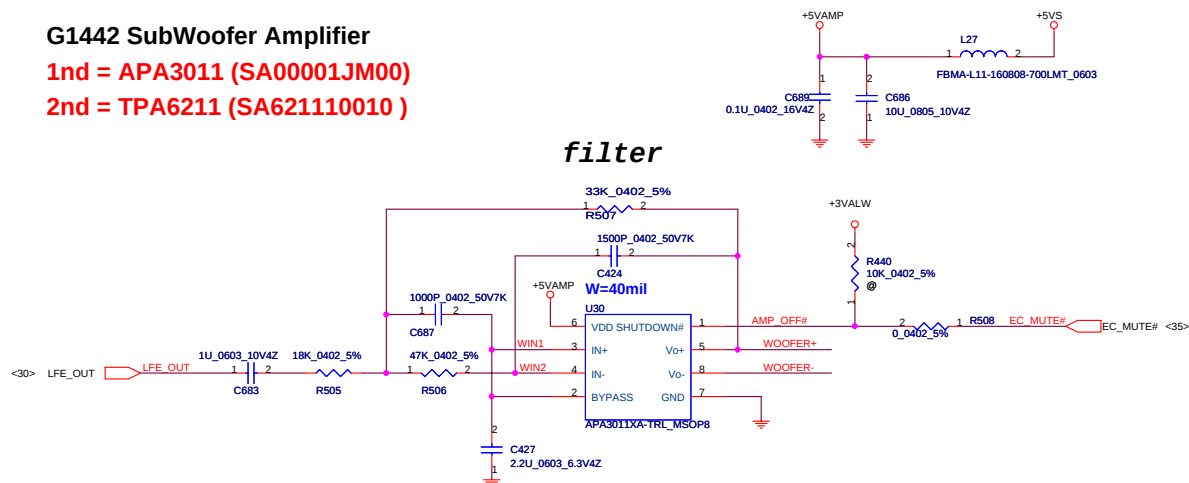
Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

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				Custom	JITRI_LA-4141P
				Date	Wednesday, May 07, 2008
				Sheet	30 of 52
				Rev	0.1

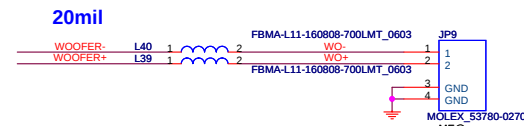
G1442 SubWoofer Amplifier

1nd = APA3011 (SA00001JM00)

2nd = TPA6211 (SA621110010)



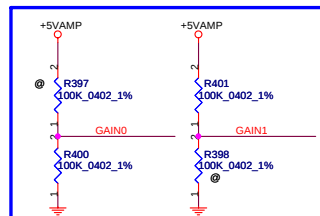
SubWoofer Conn.



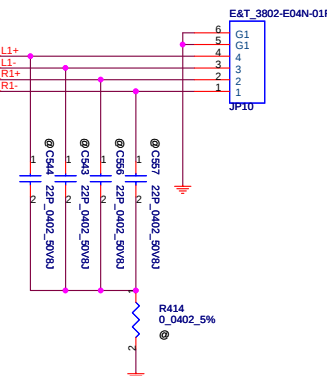
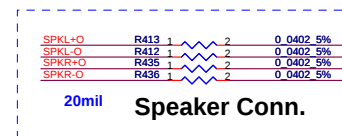
Speaker Amplifier

1nd = APA2031 (SA00001RZ00)

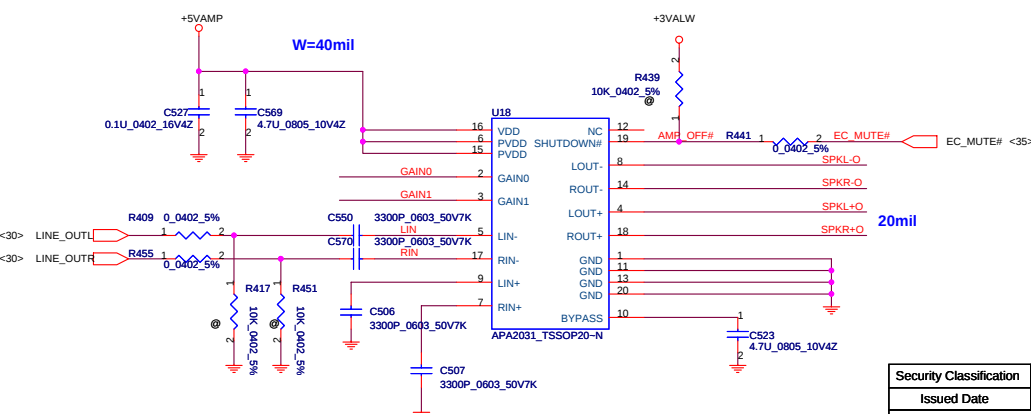
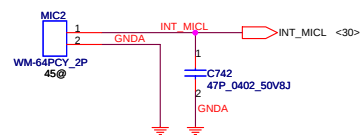
2nd = G1431F2U (SA000012Y00)



GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



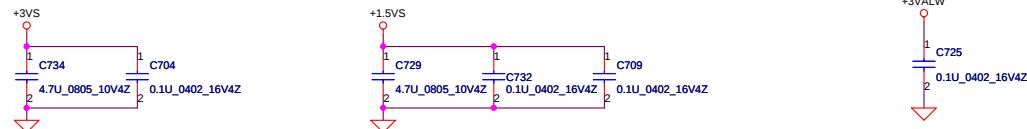
INT MIC



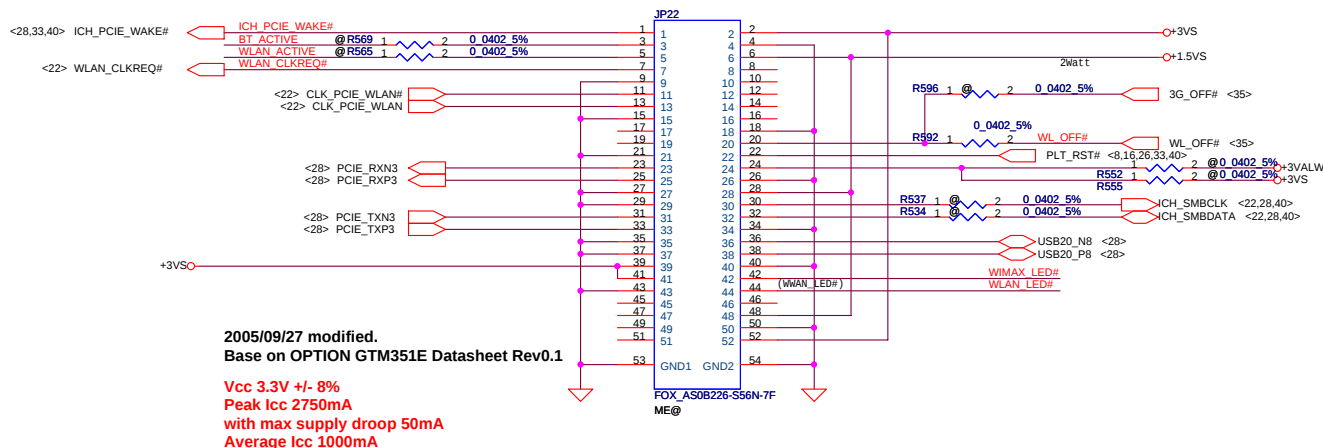
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Date: Friday, May 02, 2008				Sheet 31 of 52

Mini-Express Card for 3G Or TV Tuner

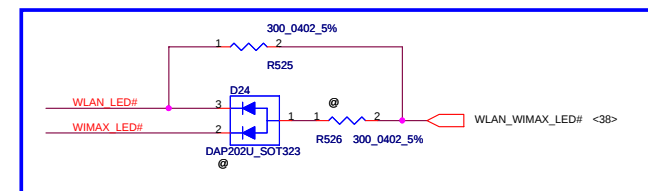
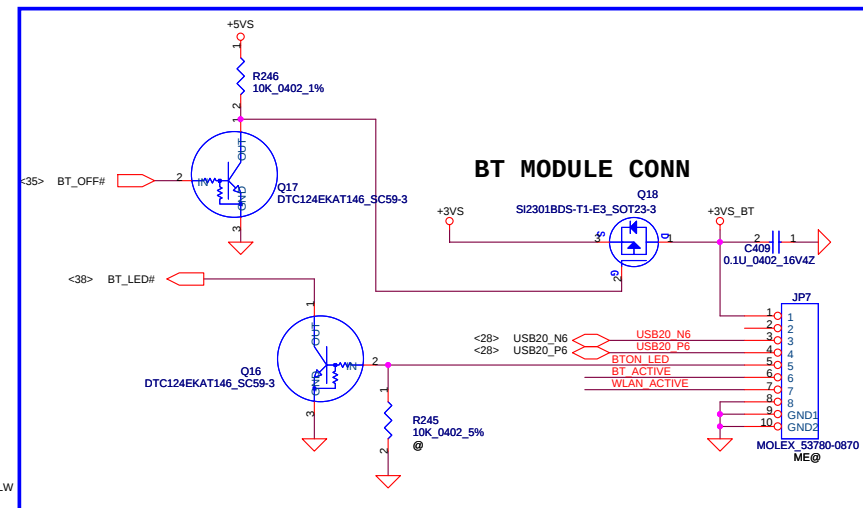
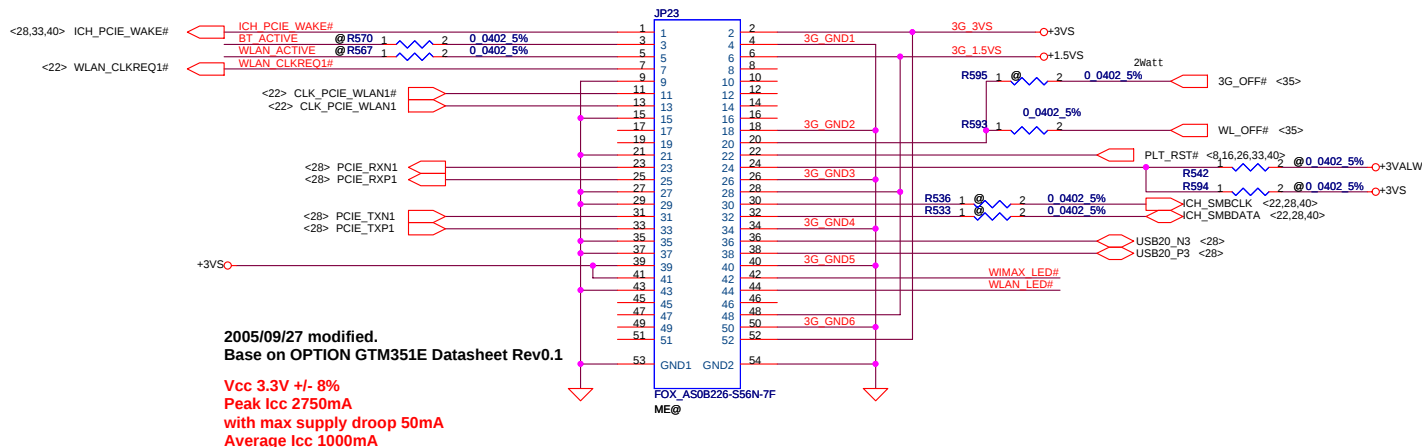
Mini-Express Card for WLAN



Mini-Express Card(Slot 1-WLAN WIMAX)

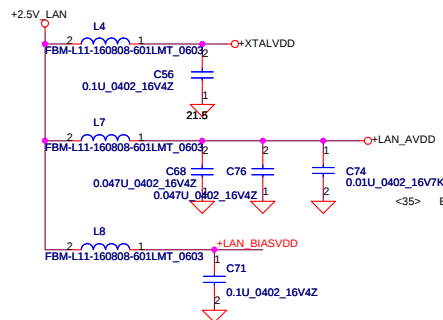


Mini-Express Card(Slot 2-WLAN WIMAX)

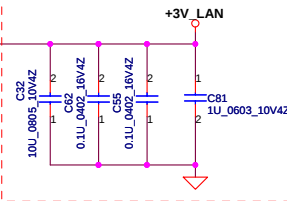


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Date: Monday, May 05, 2008		Sheet 32 of 52		Size	Document Number
				JITR1_LA-4141P	
				Rev 0.1	

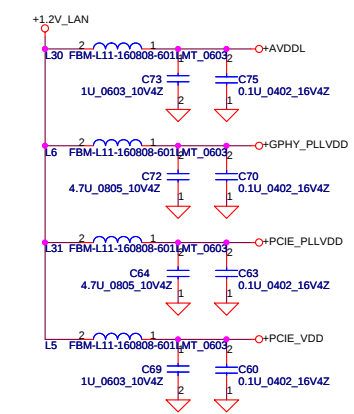
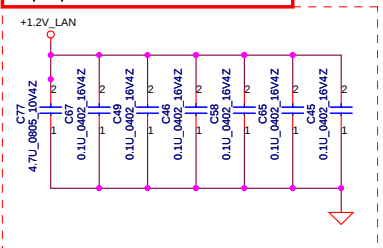
Layout Notice : Filter place as close chip as possible.



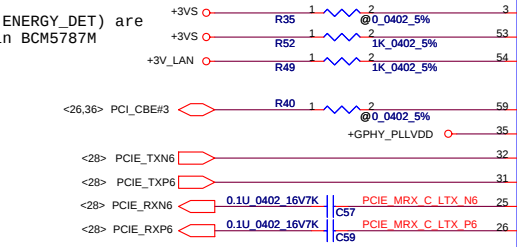
Layout Notice : Place as close chip as possible.



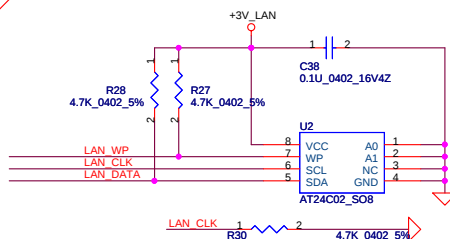
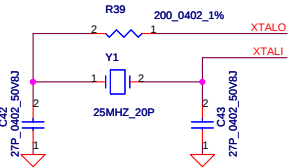
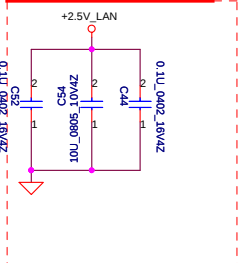
Layout Notice : 1.2V filter. Place as close chip as possible.



(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



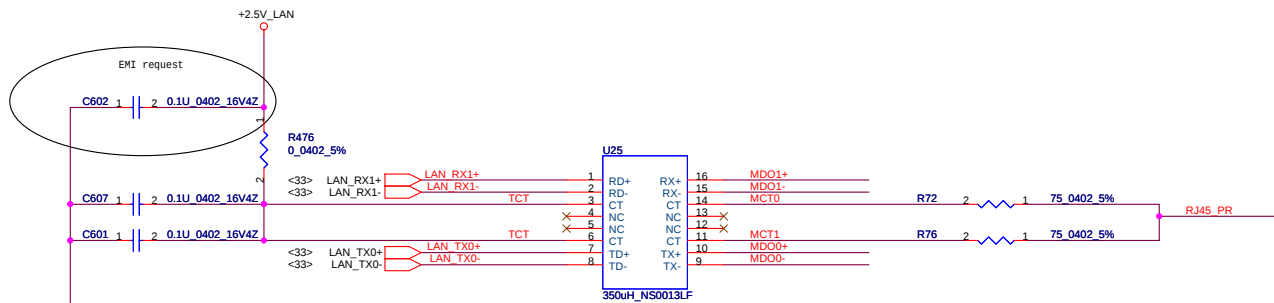
Layout Notice : Place as close chip as possible.



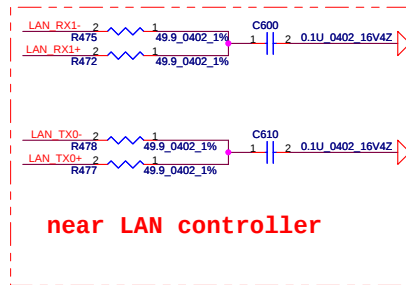
Notice : 4.7u 6.3V capacitor Thickness 1.25mm

Layout Notice : Filter place as close chip as possible.

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Size	Customer	Document Number	JITR1_LA-4141P	Rev	0.1
Date:	Friday, May 02, 2008	Sheet	33	of	52

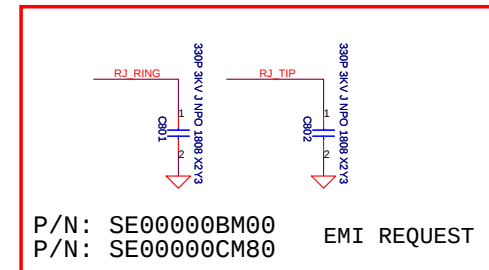
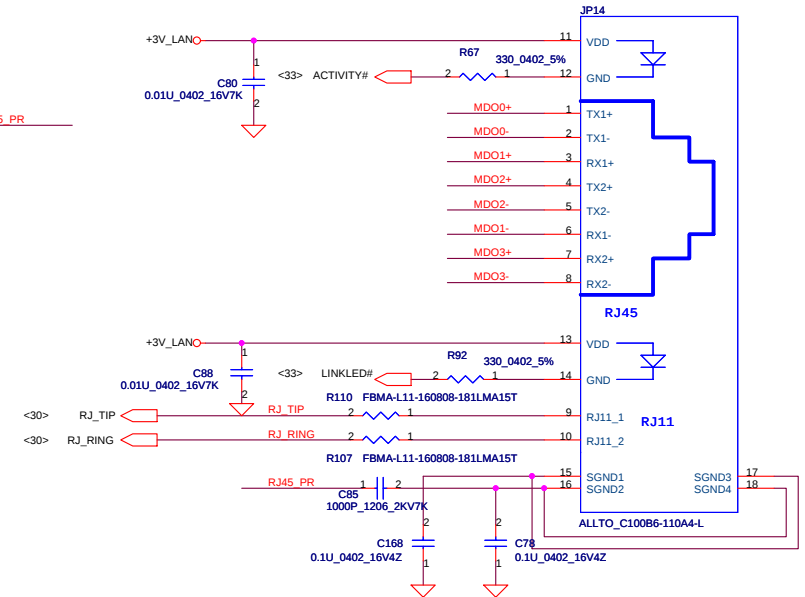


Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



near LAN controller

RJ11+RJ45 CONN



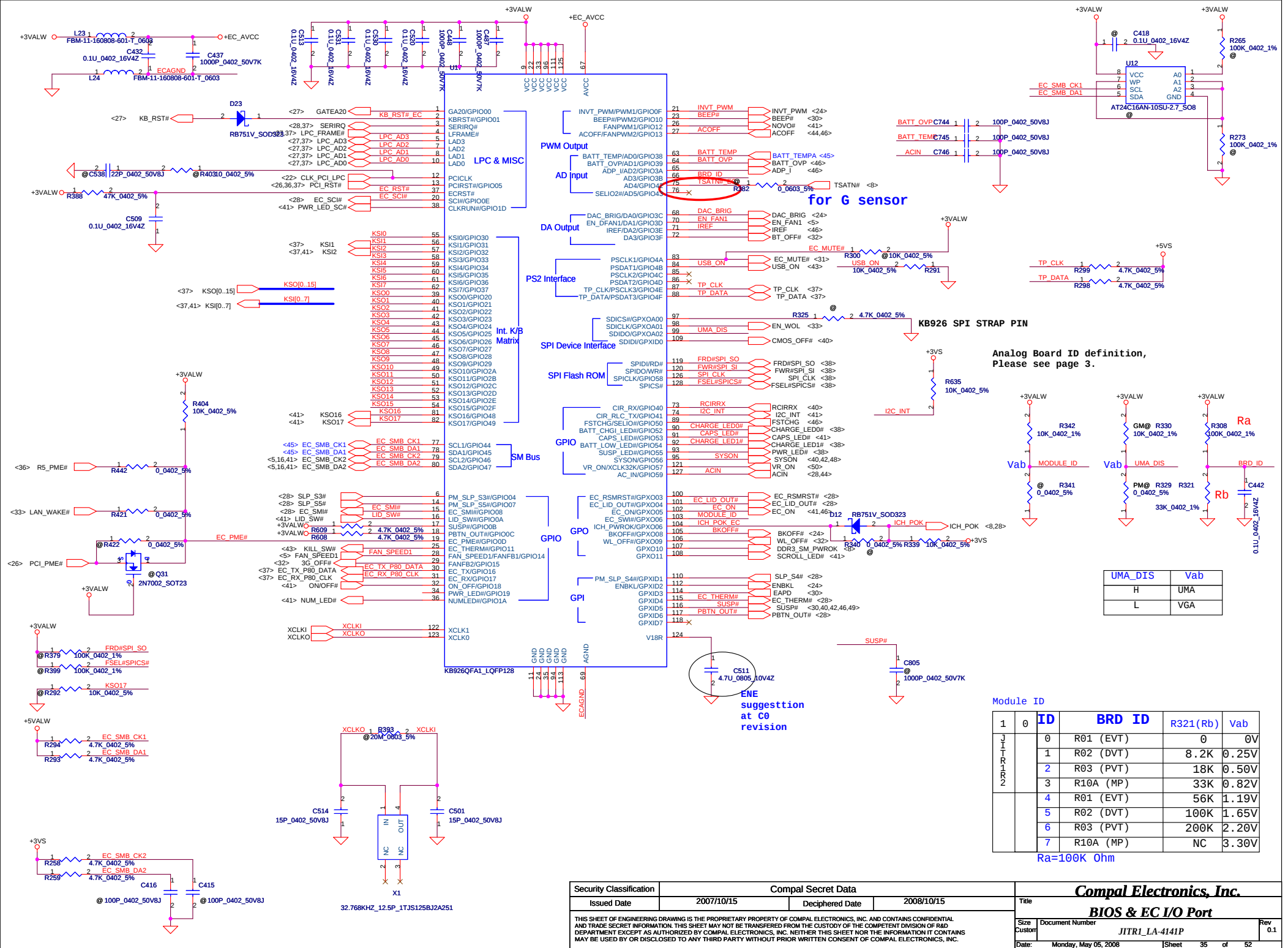
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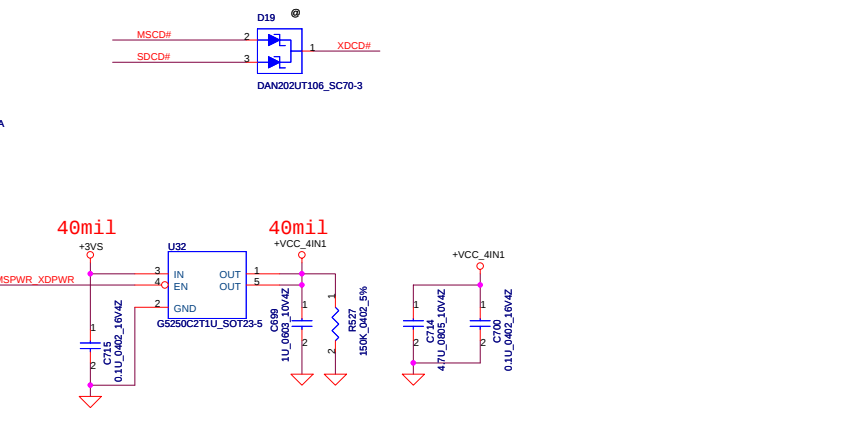
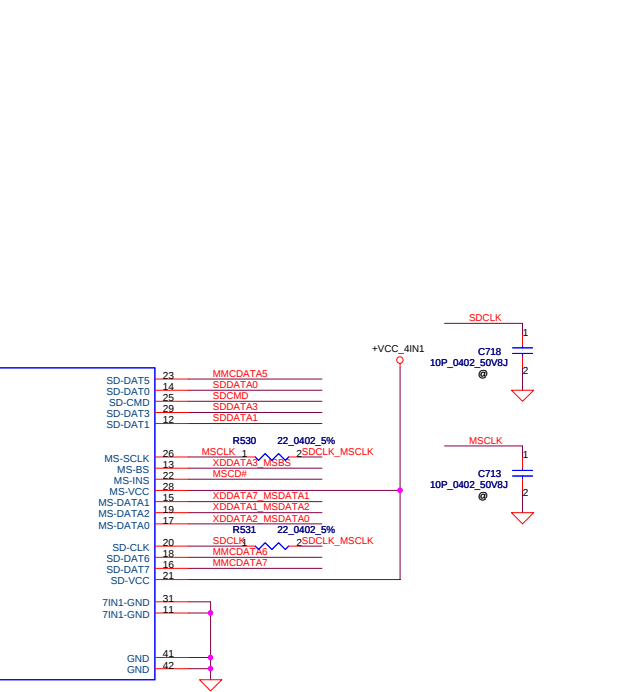
EMI REQUEST

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Deciphered Date											
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Size				Document Number				JITRI_LA-4141P			
Date:				Friday, May 02, 2008				Rev 0.1			
Sheet				34				of 52			

Compal Electronics, Inc.

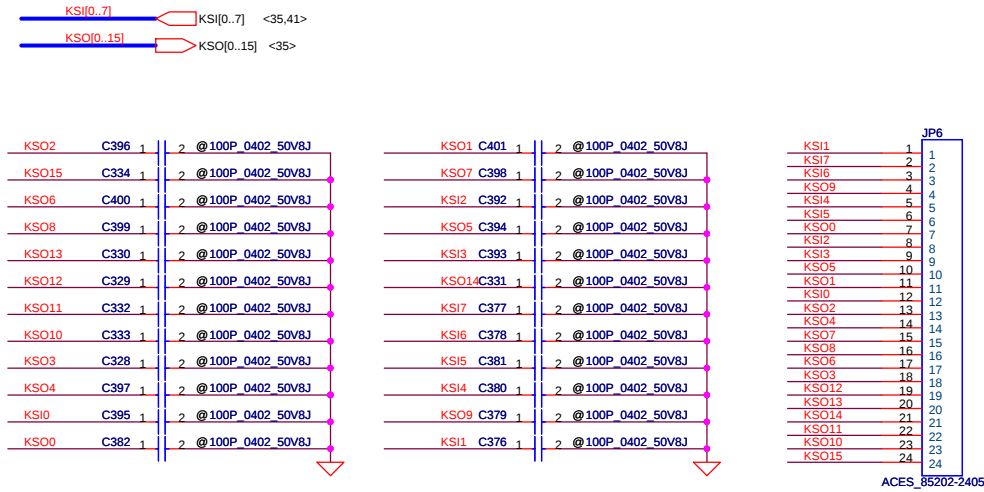
LAN CONTROLLER



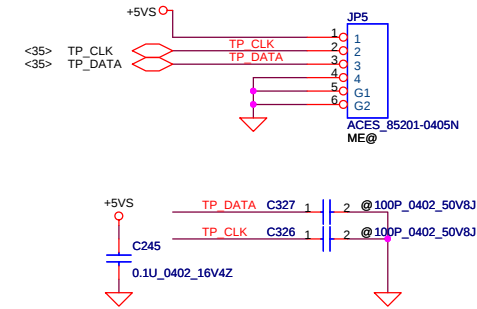


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				IGT30 LA-3571P		
				Date: Friday, May 02, 2008		Sheet 36 of 52

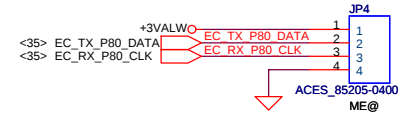
INT_KBD Conn.



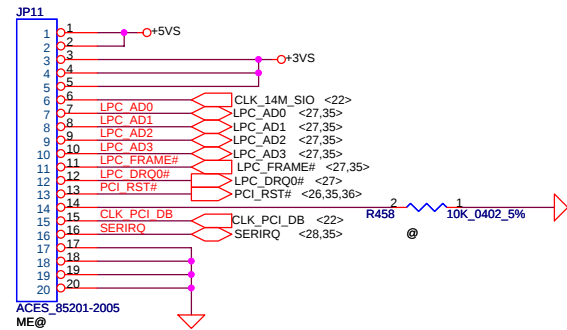
To TP/B Conn.



EC DEBUG PORT

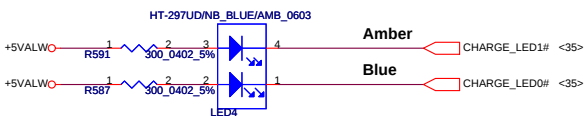
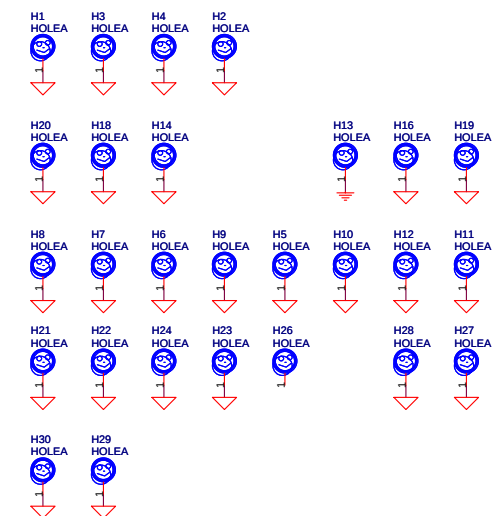
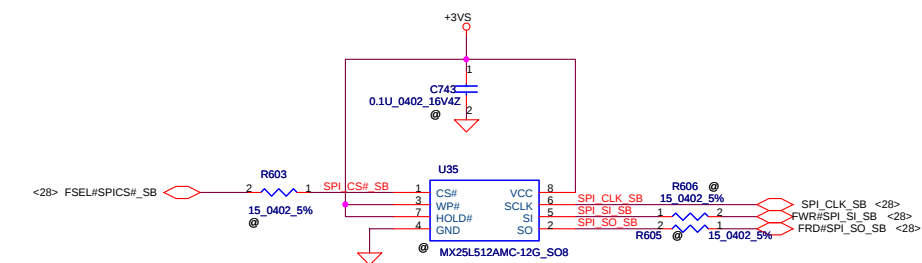


FOR LPC SIO DEBUG PORT

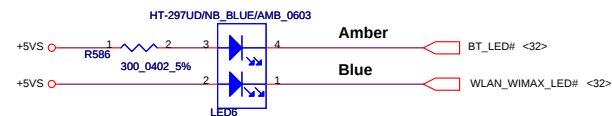


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				B	JITR1_LA-4141P
				Date	Friday, May 02, 2008
				Sheet	37 of 52
				Rev	0.1

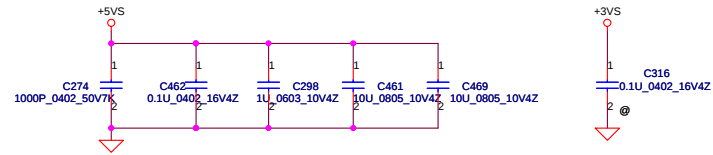
+3VALW



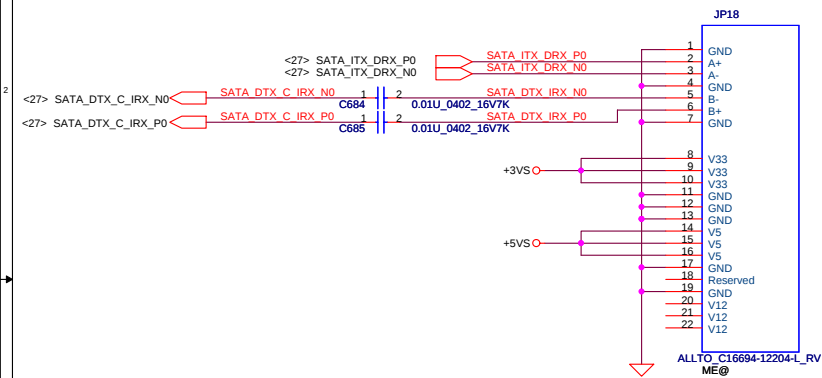
ELIUD KIPCHIRCHIR



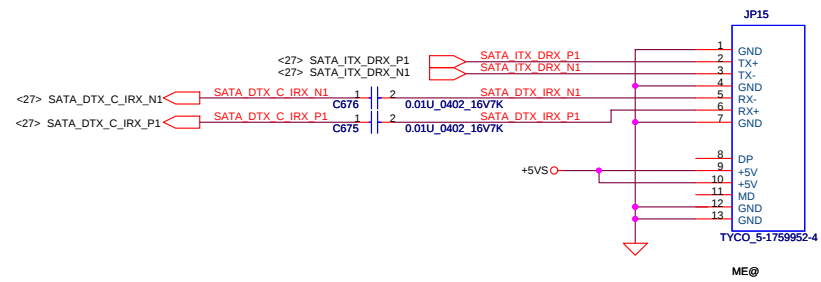
Security Classification		Compal Secret Data		Compal Electronics, Inc. LED/EC SPI ROM	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				JITRI_LA-4141P	
				Date	Monday, May 05, 2008
				Sheet	38 of 52



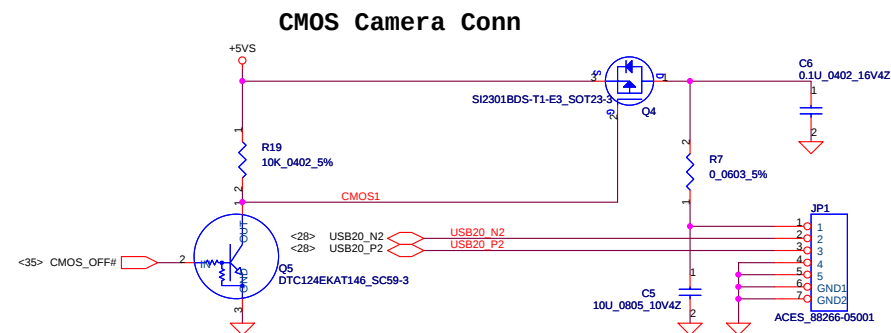
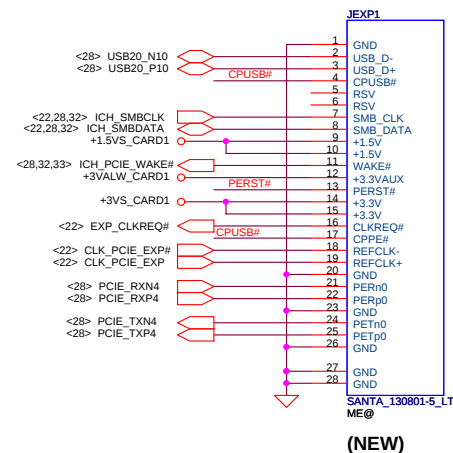
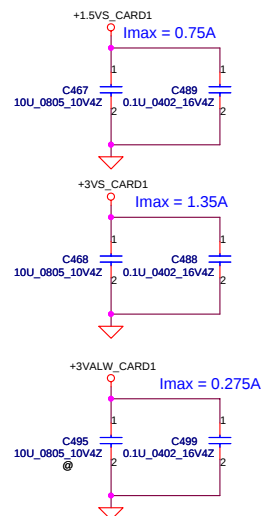
SATA HDD Conn.



SATA ODD Conn.

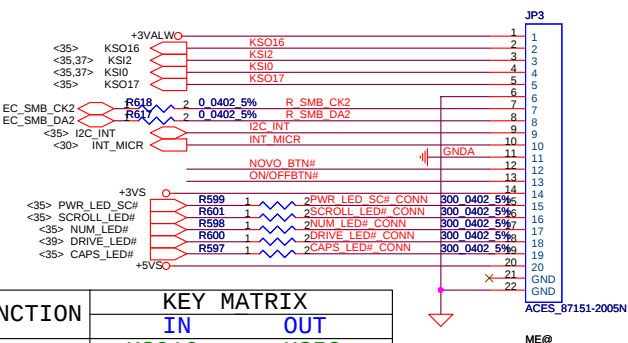


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				JITRI_LA-4141P	
Date: Friday, May 02, 2008				Rev 0.1	
[Sheet 39 of 52]					



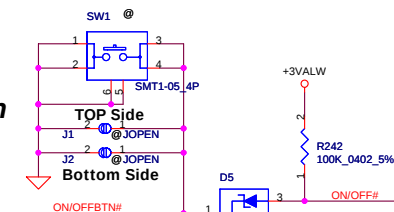
Security Classification		Compal Secret Data		Compal Electronics, Inc. NEW CARD & CMOS Connector	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Document Number	
				JITR1_LA-4141P	
Date:	Friday, May 02, 2008	Sheet	40	of	52

Switch Board Conn.

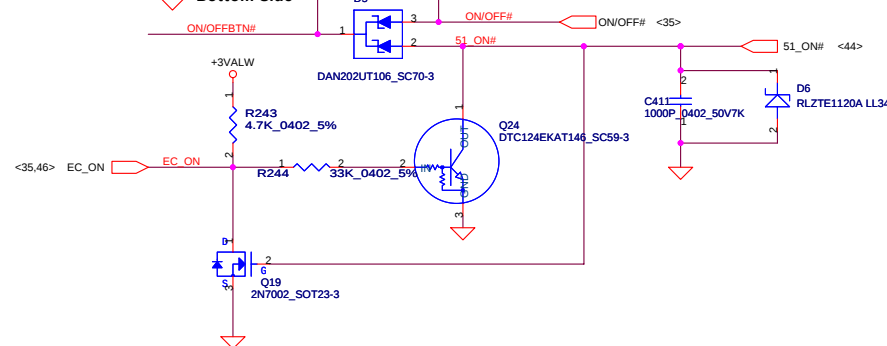


BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KS016	KS12
DOWN	KS017	KS12
OK	KS017	KS10

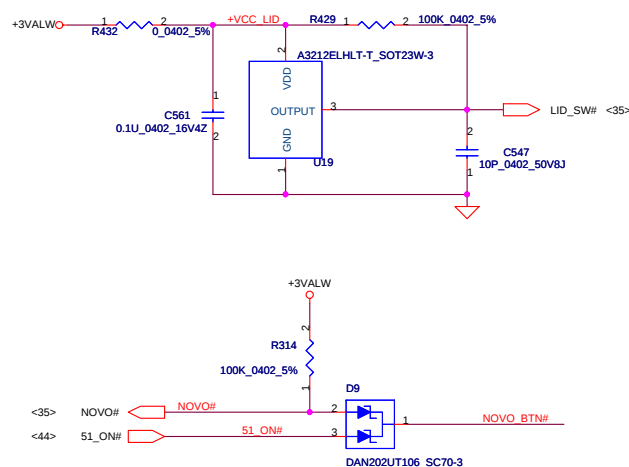
Power Button



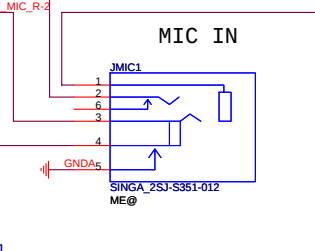
ON/OFF switch



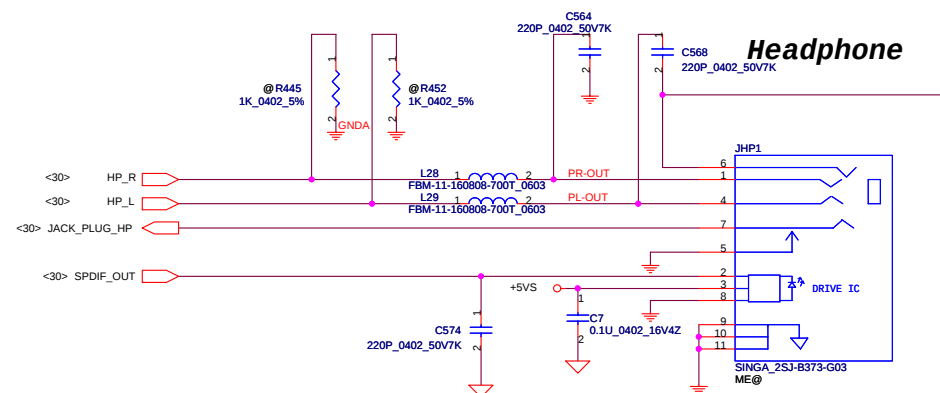
Lid Switch



Audio Jack

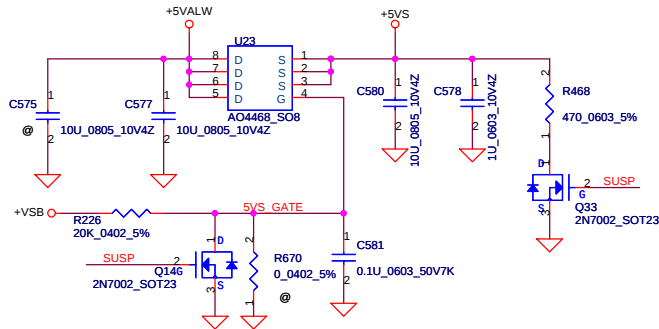


Headphone

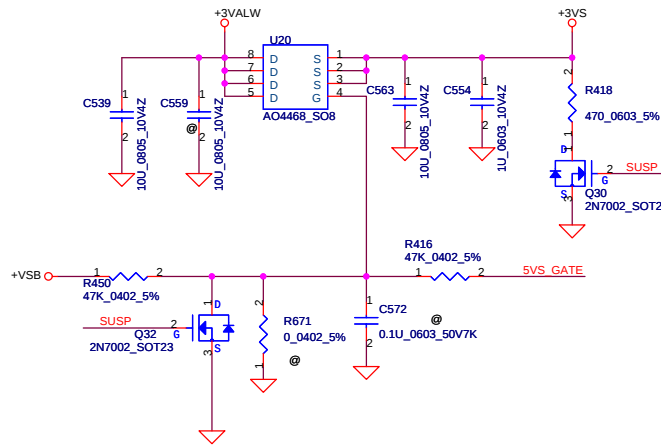


Security Classification		Compal Secret Data		Compal Electronics, Inc. Audio Jack & SW connector JITRI_LA-4141P		
Issued Date	2007/10/15	Deciphered Date	2008/10/15			
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				Date:	Mar 07 2008	Sheet 41 of 53

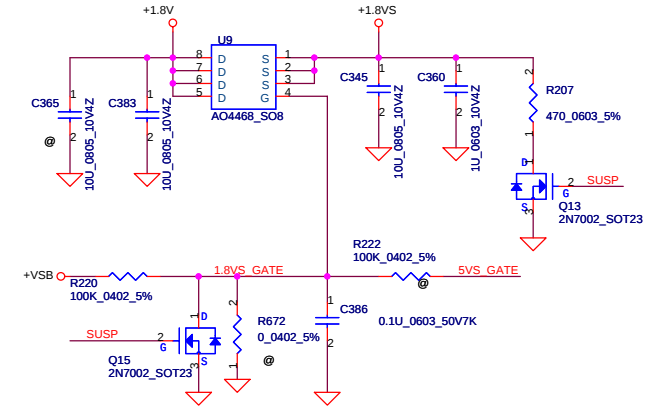
+5VALW TO +5VS



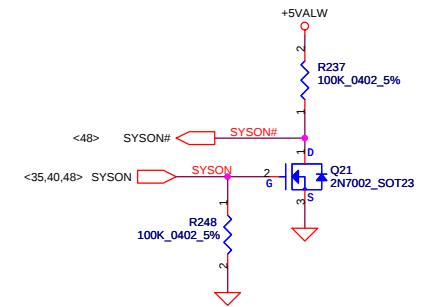
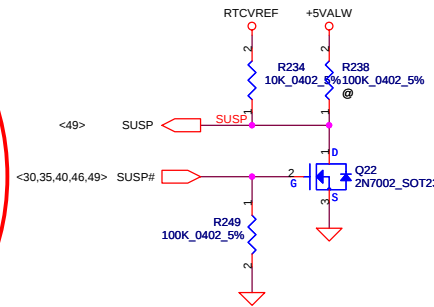
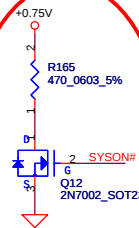
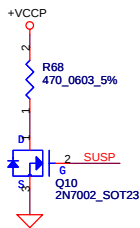
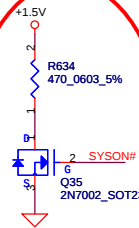
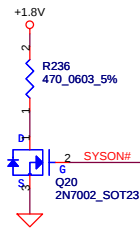
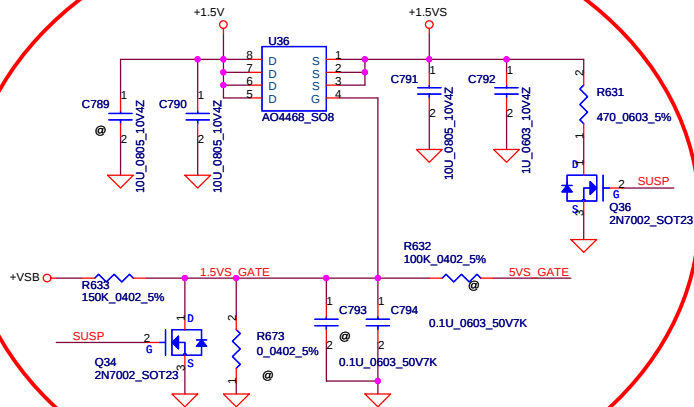
+3VALW TO +3VS



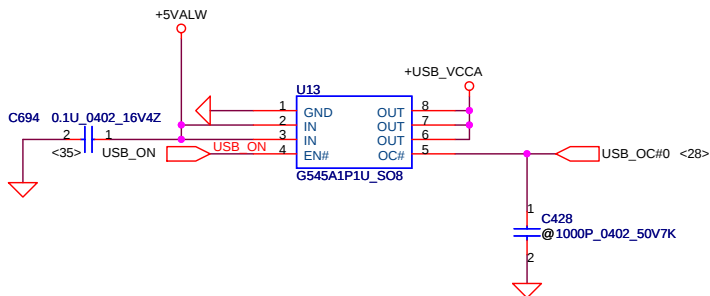
+1.8V to +1.8VS



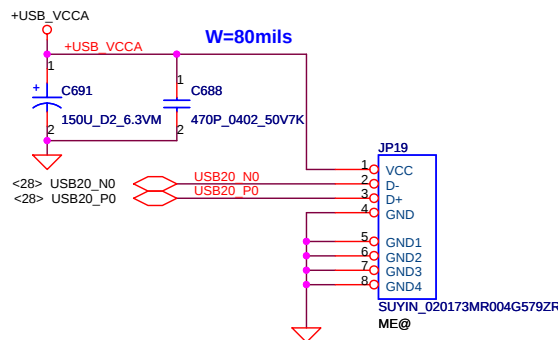
+1.5V to +1.5VS



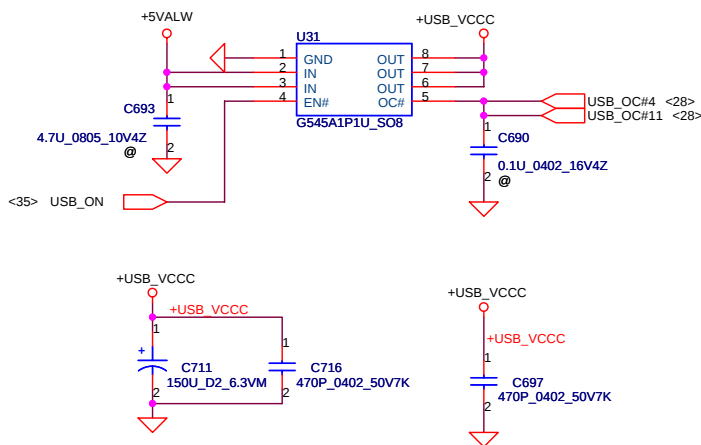
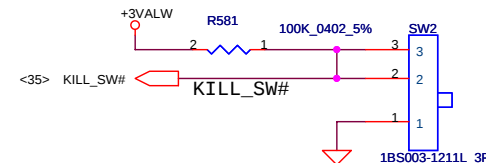
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Size	Document Number	Rev		1.0	
Date	Monday, May 05, 2008	Sheet	42 of 52	LA-3691P	



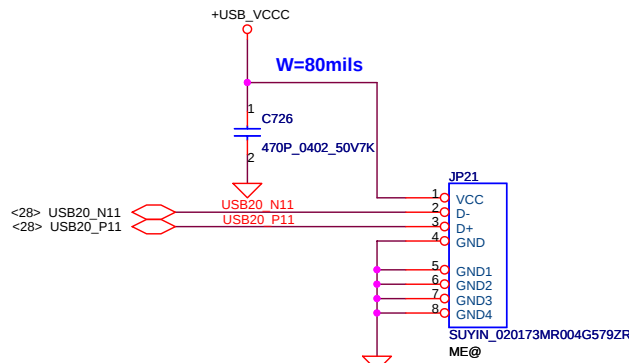
LIFT USB CONN. 1



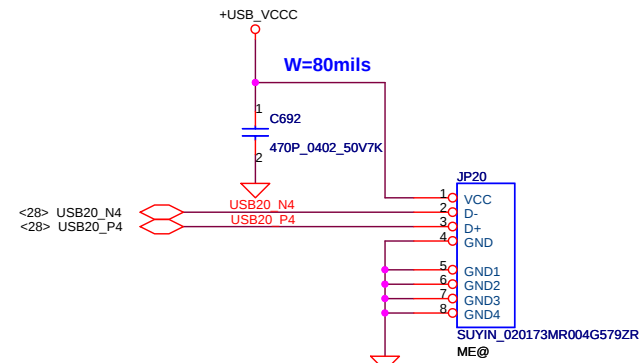
Kill Switch



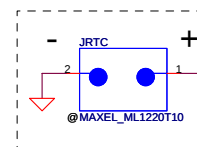
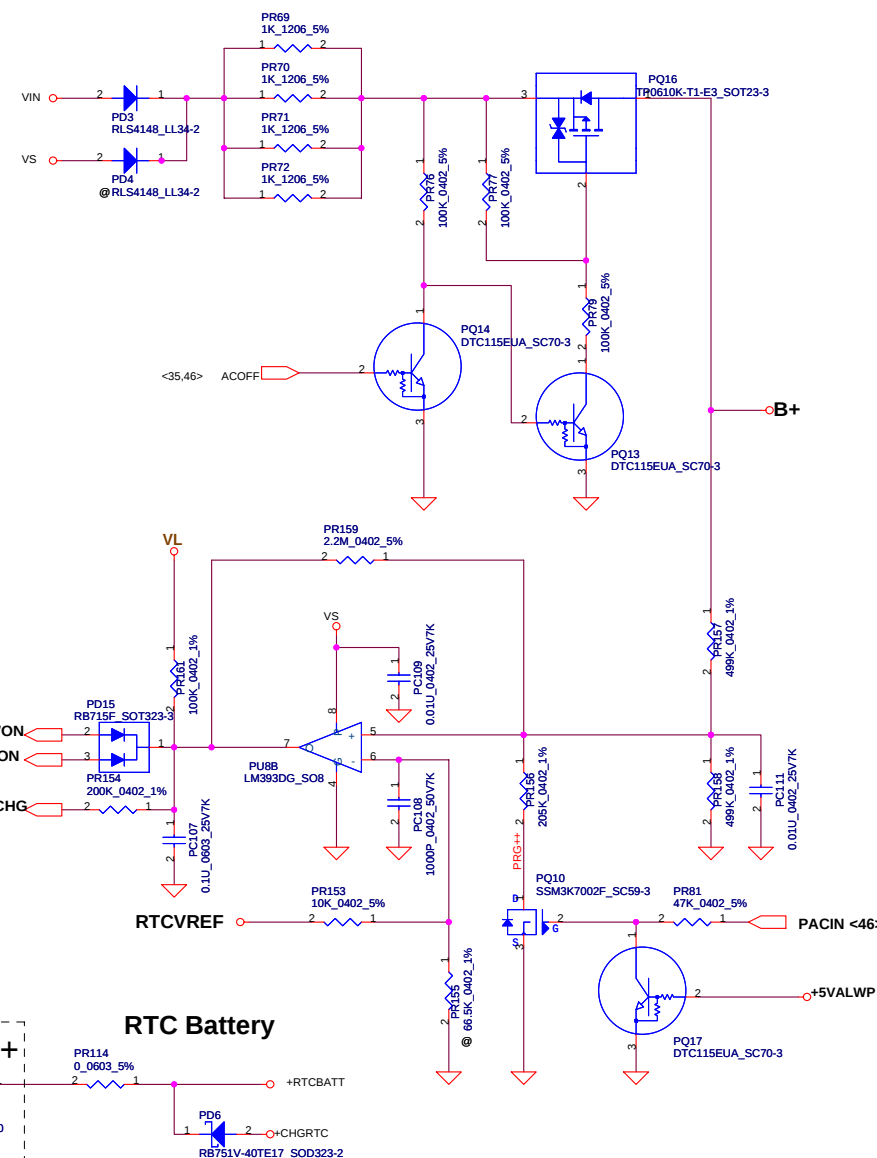
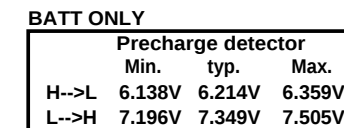
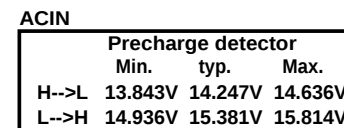
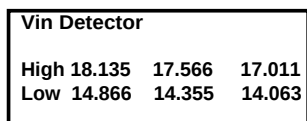
RIGHT USB CONN. 3



RIGHT USB CONN. 2

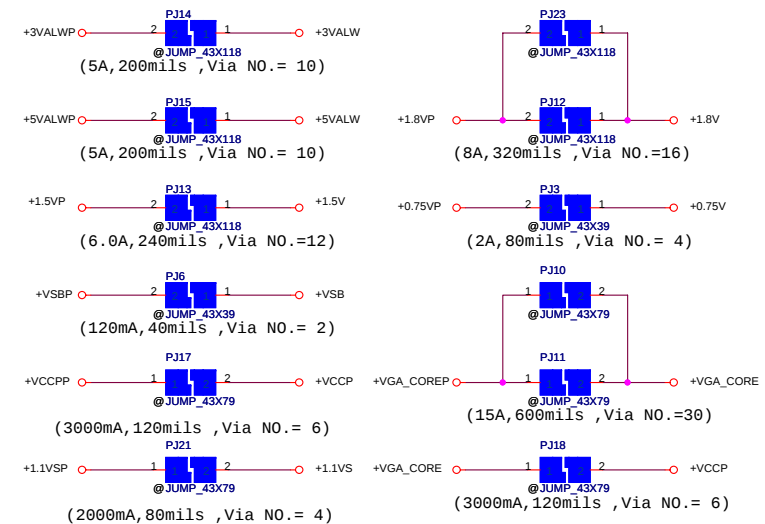
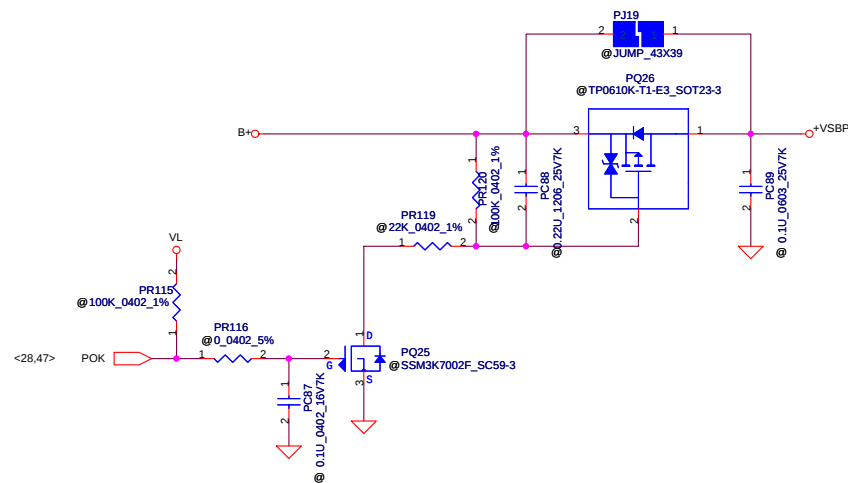
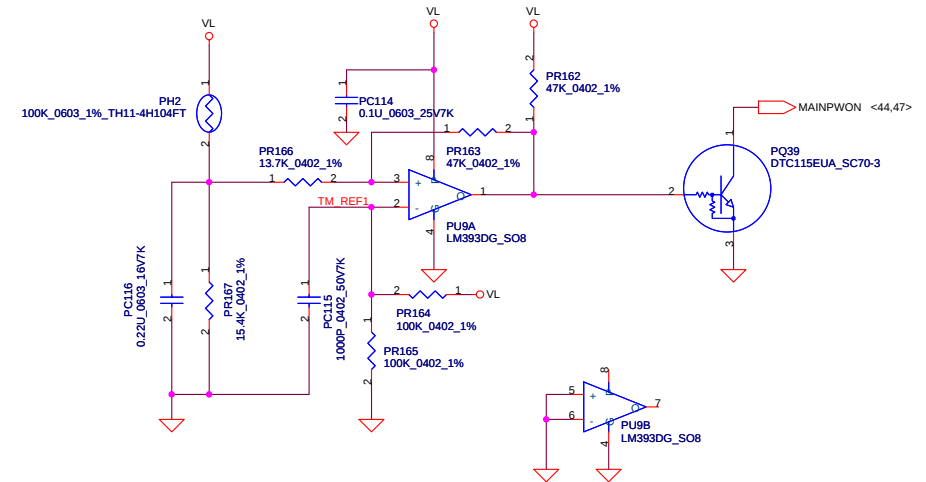
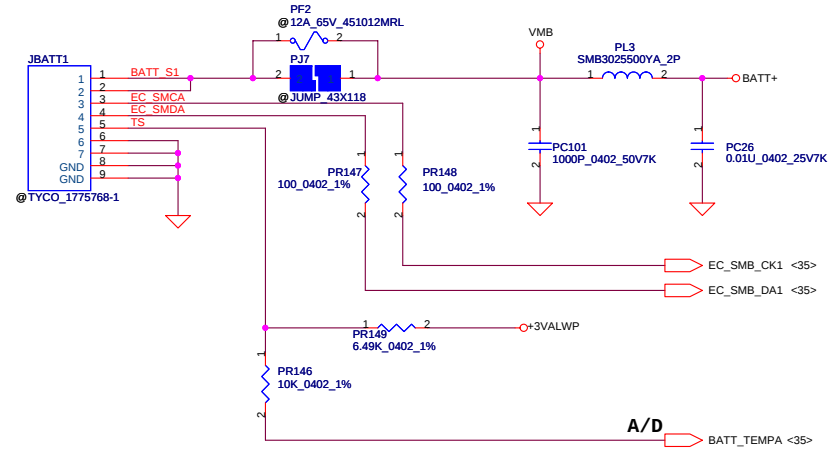


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Size	Custom	Document Number	LA-3691P	Rev	1.0
Date:	Monday, May 05, 2008	Sheet	43	of	52

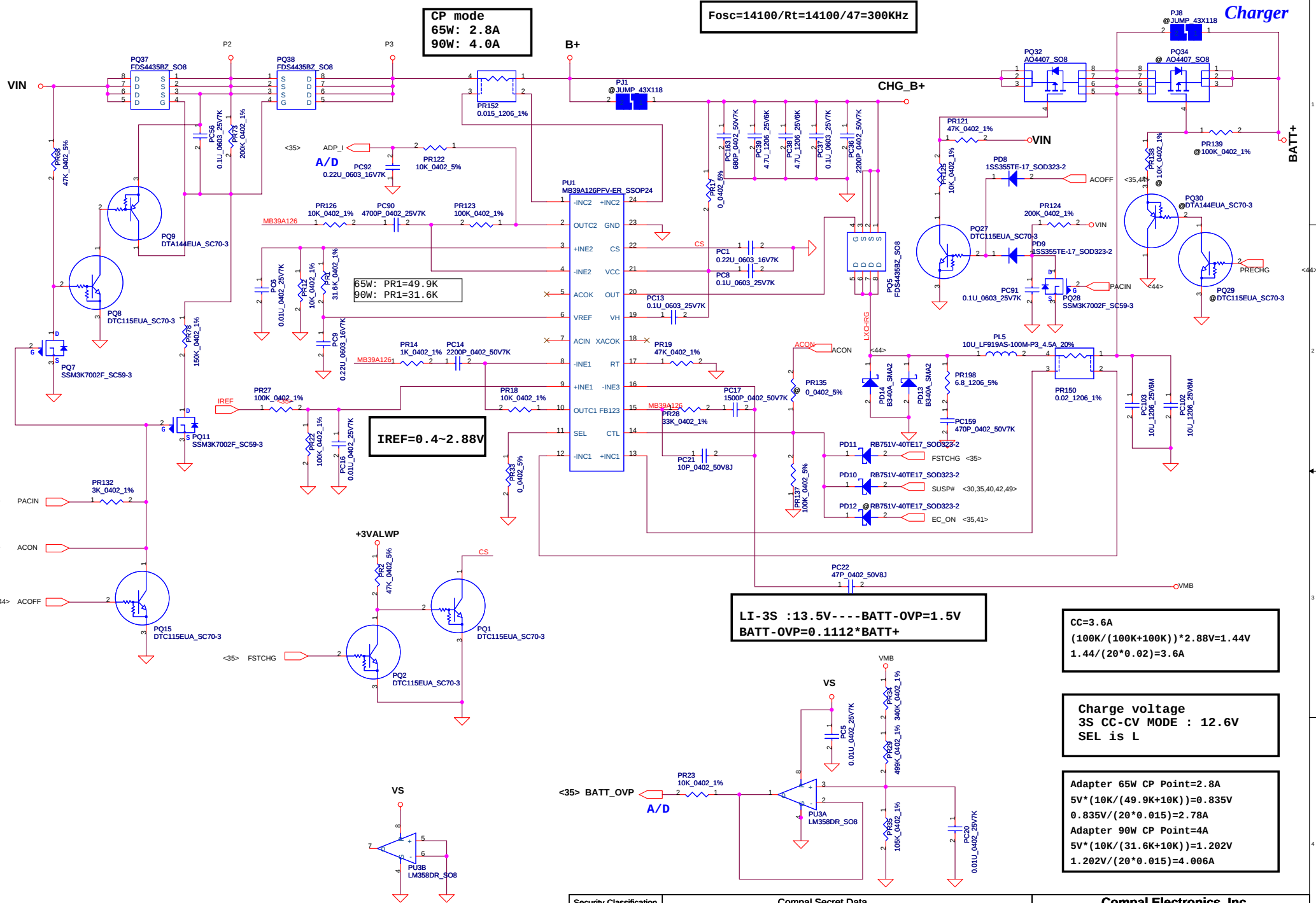


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				Size	Document Number	Rev
				Date: Friday, May 02, 2008	Sheet 44 of 52	

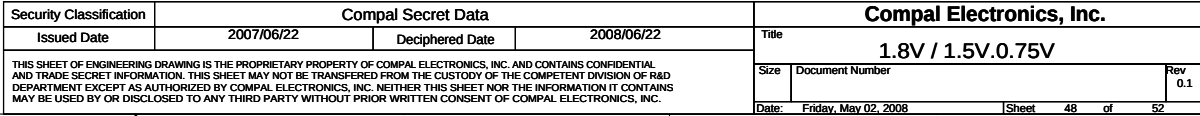
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

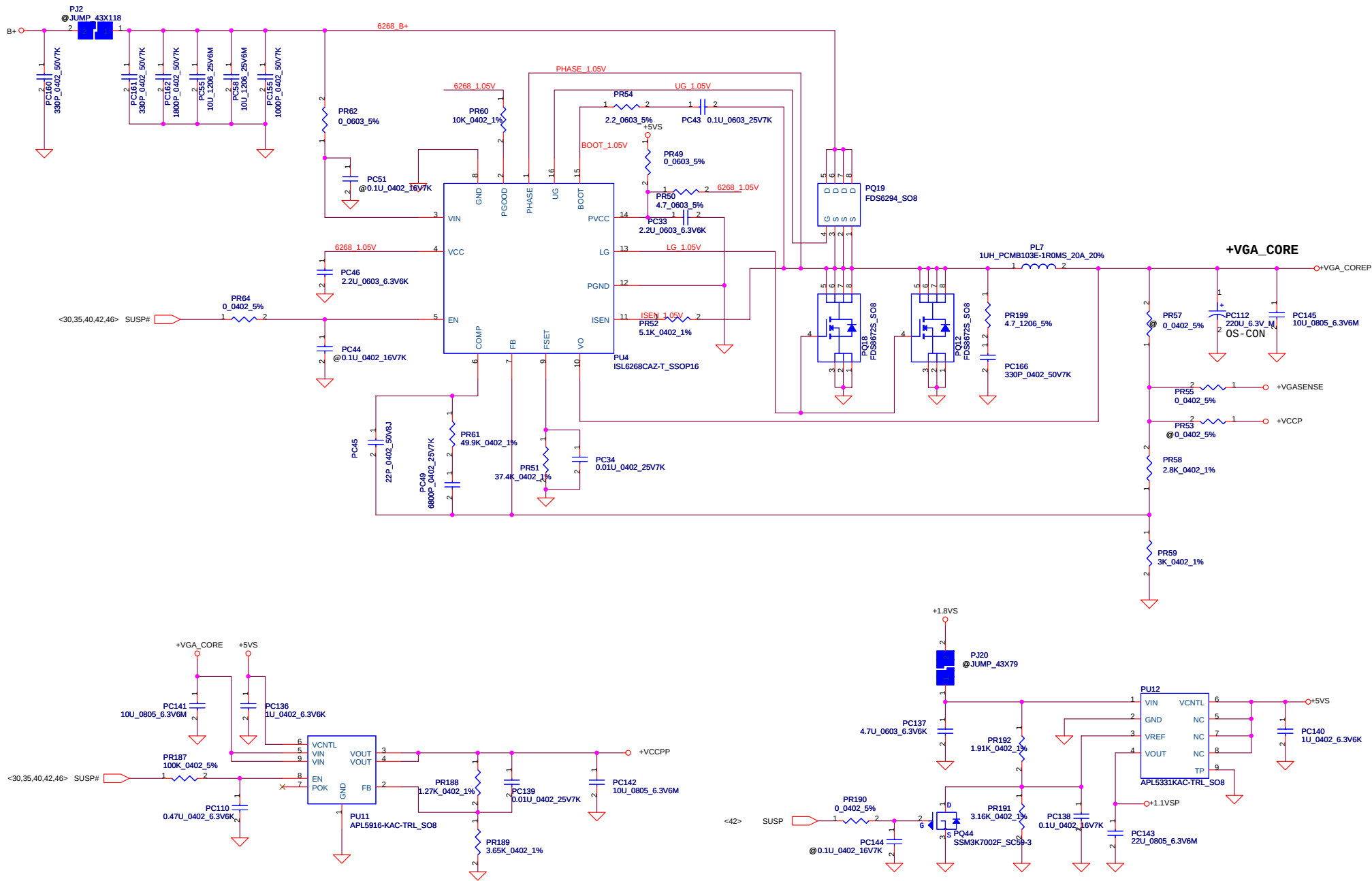


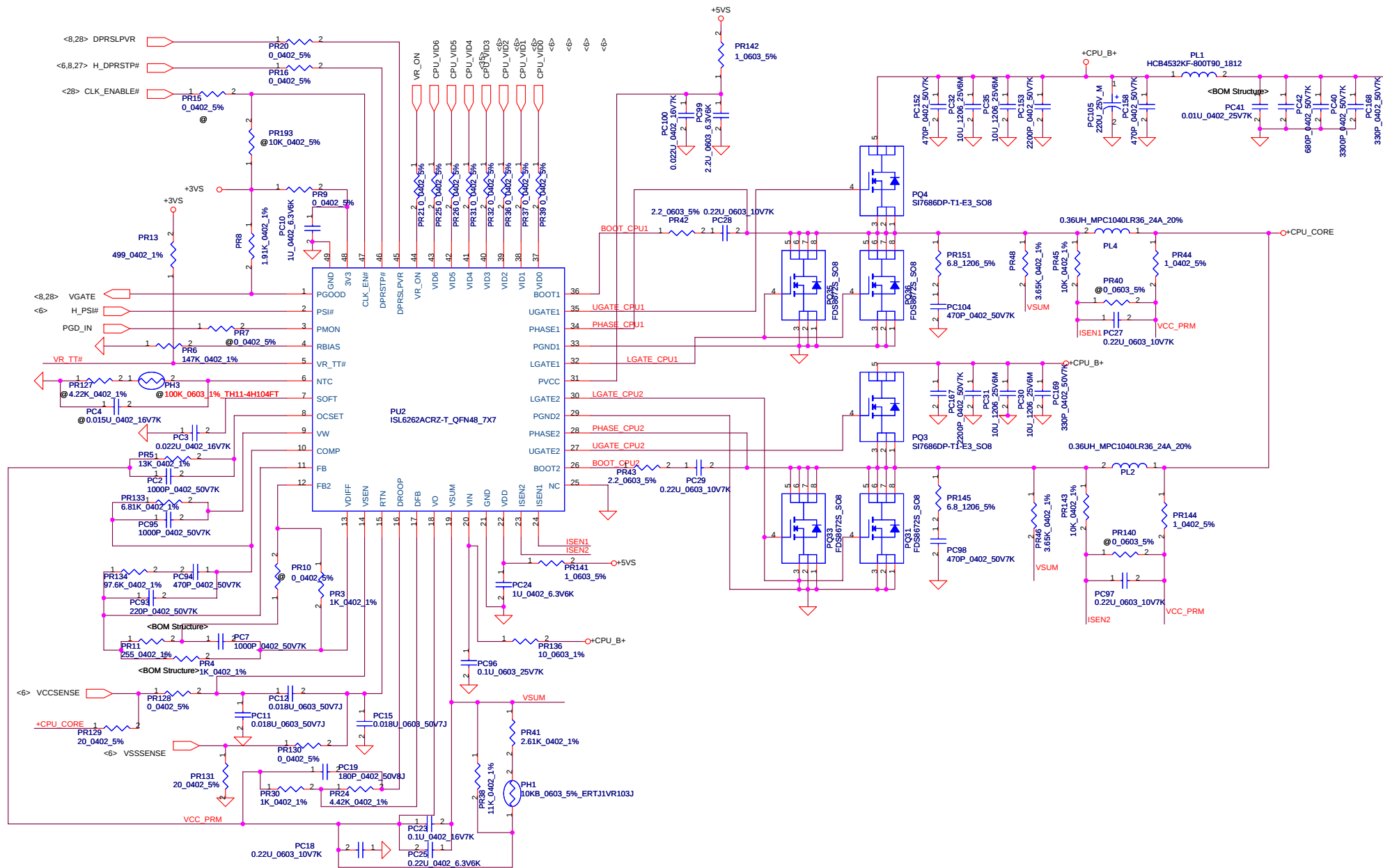
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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title	BATTERY CONN / OTP	
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				Date:	Friday, May 02, 2008	Sheet 45 of 52



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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title	CHARGER
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				Date: Friday, May 02, 2008	Rev 0.1
				Sheet 46 of 52	







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Size	Custom	Document Number	Rev 0.1	
Date:	Friday, May 02, 2008	Sheet	50	of 52

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V
11/02		P49	Add PU12, PR190, PR191, PR192, PC137, PC138, PC140, PC143, PC144, PQ44	HW request add VCCIO(1.1V) for VGA use.
11/12		P47	Add PD16, PD17	To solve 3/5VALW reboot after remove AC.
11/21		P49	Add PC145	To reduce VGA_CORE ripple.
11/21		P49	Change PR51 from 44.4k to 37.4k.	To change VGA_CORE frequency to 350KHz
12/03		P48	Add PC146	To reduce 1.8VP ripple.
12/03		P47	Add PC147	To reserve for 3/5V IC 2nd source.
12/17		P48	Change PR105 from 16.9k_0402_1% to 16.5k_0402_1%, PR96 from 16.9k_0402_1% to 22k_0402_1%, PR93 from 25.5k_0402_1% to 34.8k_0402_1%.	Adjust 1.5V to 1.549V, 1.8V to 1.8V to 1.865V
12/17		P48	Add PC148.	Reserve for HW adjust power sequence.
12/27		P47, P48, P49, P50	Add PC149, PC150, PC152, PC153, PC155, PC151, PC154, PC156, PC157, PC158, PR194, PR195, PR196, PR197	For EMI request, to decrease power broadband.
12/31		P49	Change PR58 from 2.8k_0402_1% to 3k_0402_1% PR188 from 1.27k_0402_1% to 1.4k_0402_1%.	For intel request, ES2 NB need adjust VCCP to 1.1V.
02/29		P46	Add PR198, PC159.	Reserve charger sunbber.
02/29		P46	Change PR192 from 1.87k_0402_1% to 1.91k_0402_1%.	HW request adjust 1.1V to 1.12V.
02/29		P49	Change PR64 from 0_0402_5% to 100k_0402_1%, PC44 to 0.47u.	HW adjust power sequence.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI requesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
04/29		P50	Add PC167, PC168, PC169	For EMI request, to decrease power broadband.

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Title						
Power PIR						
Size						
Document Number						
LA-4141P						
Rev						
0.1						
Date						
Tuesday, April 29, 2008						
Sheet						
51 of 51						

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